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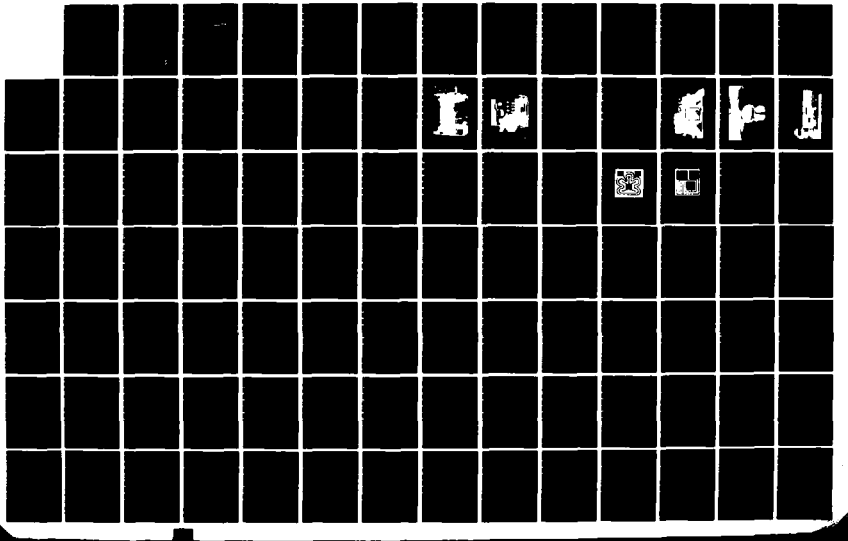

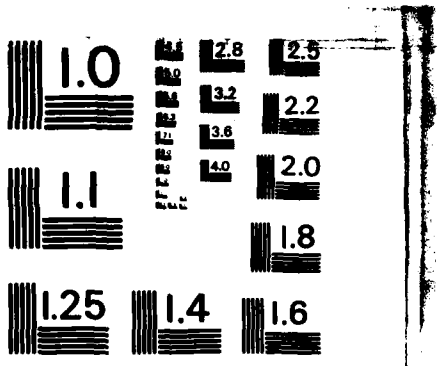

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A PROBE FOR MEASURING SPACECRAFT SURFACE POTENTIALS USING A DIRECT-GATE FIELD EFFECT TRANSISTOR

Mark N. Horenstein
Anton Mavretic

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) Experimental research aimed at the development of a solid state electrostatic field and surface potential sensor has been performed. The overall goal has been to obtain a sensor that overcomes the deficiencies of existing field sensors, including the need for mechanical moving parts and relatively high power consumption.

As a result, both the Floating Gate Field Effect Transistor (FGFET) and Direct Gate Field Effect Transistor (DGFET) have been developed and tested. Both devices have been successfully used to measure electrostatic fields over extended periods of time on the order of hours, and a plausible theory for

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device behavior has been formulated and corroborated with experimental data.

Device shortcomings include substantial sensitivity to temperature changes and to extraneous sources of light (DGFET). A moderate amount of random operating point drift has also been observed.

Both FGFET and DGFET devices have been incorporated into a complete 0-20 kV electric field and surface potential measuring system, which includes a probe head electrode for each type of sensor, a synchronous detector system (to allow for potentials down to the 200 Volt range to be monitored), and a thermal control system, which can hold the temperature of the sensor to within ±2°C of a specified set point temperature.

0. SUMMARY

Experimental research aimed at the development of a solid state electrostatic field and surface potential sensor has been performed. The overall goal has been to obtain a sensor that overcomes the deficiencies of existing field sensors, including the need for mechanical moving parts and relatively high power consumption.

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A Probe for Measuring Spacecraft Surface Potentials
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1. INTRODUCTION

The charging of spacecraft at high altitudes by photon or plasma fluxes has been recognized by many investigators as a serious problem that effects many types of communications, research, and strategic satellites [4,6,7,9]. Charging can occur [6,4] when a satellite encounters a plasma flux, as the plasma electrons, which are the most energetic plasma particles, begin to charge the various parts of the satellite negatively relative to the plasma potential. Charging of the spacecraft relative to the plasma potential may result in the creation of large potential differences across insulated portions of the satellite [1,6]. If a given potential difference is high enough, an arc discharge may occur across an insulating surface or volume, resulting in the generation of electromagnetic pulses and high discharge currents which can damage insulating materials and sensitive electronic circuitry onboard the spacecraft, generate false logic command signals, or possibly injure personnel aboard manned vehicles [4].

The analysis and control of spacecraft charging phenomena requires the use of instrumentation that can measure the electrostatic potential of charged spacecraft surfaces. The purpose of the work cited in this report has been to investigate the development of a completely solid state dc electrostatic field sensor, that could be used as part of a spacecraft monitoring instrument, or as a component in an active spacecraft discharge

system.

1.1 Goals of the Research Project

The measuring of electrostatic fields and potentials has traditionally been one of the more difficult problems in the physical sciences. Because electrostatic potentials are created by fixed, static charges, attempting to measure such potentials with conventional high impedance voltmeters invariably leads to extreme source loading, and erroneous results. If the charged surface is made of insulating rather than conducting material, the problem is even more acute, because the location at which the surface must be "probed" becomes ambiguous.

One traditional method for measuring dc surface potentials in a non-contacting manner involves modulating the capacitance between the surface to be measured and a sampling electrode held in close proximity to the surface [11]. The modulation, which must be accomplished by a mechanically vibrating reed or rotating vane, induces on the sampling electrode an ac current proportional to the static field being measured. Knowledge of the modulation, or "chopping" speed, as well as induced electrode current, leads to a value for the dc surface field. The disadvantage of such a system lies in the mechanically moving member, which can be unreliable, and in the relatively large amount of power required to drive it. For the remote environments of space, mechanically based sensors are less than optimal.

The inherent deficiencies of existing dc field sensing techniques has motivated the goals of the research reported

here. From the outset, our approach to field sensing has centered around utilization of the metal-oxide-semiconductor field effect transistor (MOSFET), a device in which a metal "gate" electrode is insulated from the surface of a semiconducting substrate by a thin, insulating oxide layer [2,3]. Because current loading by the gate of the MOSFET is minimal, these devices are well suited for measuring the static fields associated with insulated distributions of charge. In normal usage, the gate lead of the MOSFET transistor is connected to a field sampling electrode which is capacitively coupled, without physical or electrical contact, to the surface potential being measured. A build up or change in the monitored surface potential thus causes an induced change in the MOSFET gate voltage, with corresponding changes in the MOSFET drain to source current.

Although the MOSFET sensor obviates the need for mechanical parts, it is not without its disadvantages. For example, a MOSFET with external gate connections is very susceptible to oxide layer puncture from stray electrostatic discharge (ESD) because of large voltages induced between the connections to the gate and circuit ground, or because of charge buildup on the external gate circuitry. More importantly, however, the capacitively coupled MOSFET is not capable of measuring truly dc fields. Rather, because of the nature of capacitive coupling, it can only measure the transients associated with changes in the field. Fortunately, the turn on or build up of a given dc surface potential, if it occurs fast enough, will appear as an initial, measurable transient to a capacitively coupled MOSFET.

However, once such a surface potential has reached a constant value, the capability of the MOSFET sensor begins to degrade. Left to monitor a constant dc field or potential for an indefinite period of time, the MOSFET with electrostatically induced gate voltage will eventually relax to the zero field state by the mechanism of charge relaxation, which will occur within the gate electrode structure. In particular, stray leakage resistances that are in contact with the insulated gate electrode will cause any capacitively induced gate voltage to decay to zero.

Noting the drawbacks discussed above, the overall goal of the research reported here has been to improve the MOSFET sensor by the elimination of external gate connections. By creating a device in which the gate electrode is directly coupled to the static field, without an external electrode, the hazard of ESD can be greatly reduced. Similarly, elimination of the external electrode greatly increases the magnitude of the resistive leakage paths, and hence the relaxation time of the gate electrode, thereby greatly enhancing the time over which a given sensor can monitor electrostatic fields.

1.2 Overview of Research Efforts

With the overall goal of sensor improvement cited in the previous section in mind, four basic phases of research activity were initiated. First, initial tests were made on standard MOSFET's configured as field sensors, so that a large body of data could be gathered for comparison with later experiments.

The basic electrode configuration used for the test is shown in Figure 1.1, where an external, insulated sampling electrode is incorporated into a parallel plate system. With the completion of these experiments, efforts next focused on the development of the Floating Gate Field Effect Transistor (FGFET). This device, which is pictured systematically in Figure 1.2, consists of a standard MOSFET chip (external transistor case cover removed), with the bonding wire to the gate severed at the gate electrode pad. The gate electrode, thus left electrically floating, is subject to direct exposure to external electrical fields. The inherent properties of this device, even with no field present, are very interesting, and will be described in Section 3.2. The FGFET's basic advantages as a field sensor lie in the greatly reduced leakage paths to its gate electrode, and in its likely reduced susceptibility to ESD damage.

In an attempt to further improve on the FGFET sensor, efforts were also directed to the development of a MOSFET device with no gate electrode at all. In the Direct Gate Field Effect Transistor, or DGFET, shown in Fig 1.3, the field to be measured is allowed to land directly on the FET substrate, through the oxide layer, with no gate electrode intervening. The surface leakage paths that contribute to relaxation processes are thus physically longer t[illegible]hose of the FGFET. At the same time, the danger of oxide la[illegible]re is minimal, and possibly not catastrophic, since [illegible]te electrode exists.

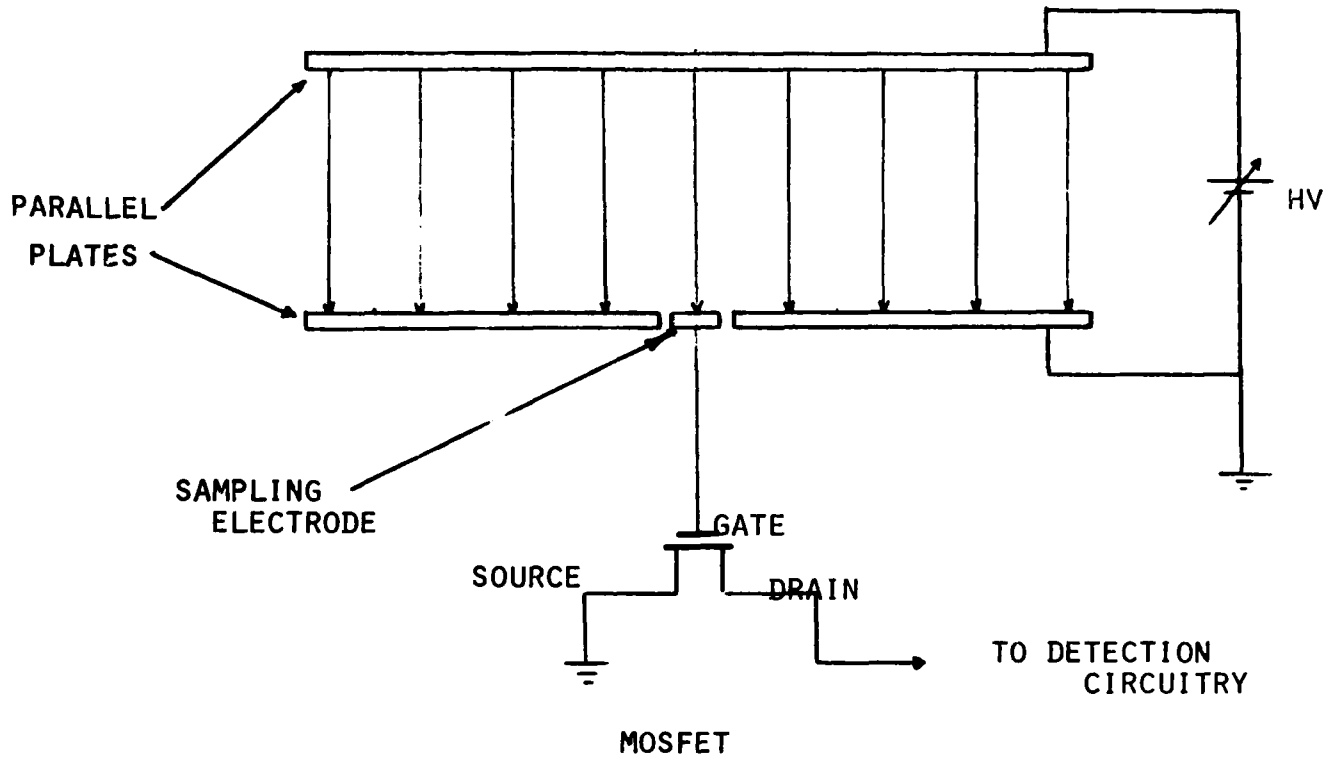


Figure 1.1 Schematic view of electrode configuration used for testing unmodified MOSFETS. The upper plate, energized to high voltage, creates a uniform field in the neighborhood of the external gate sampling electrode.

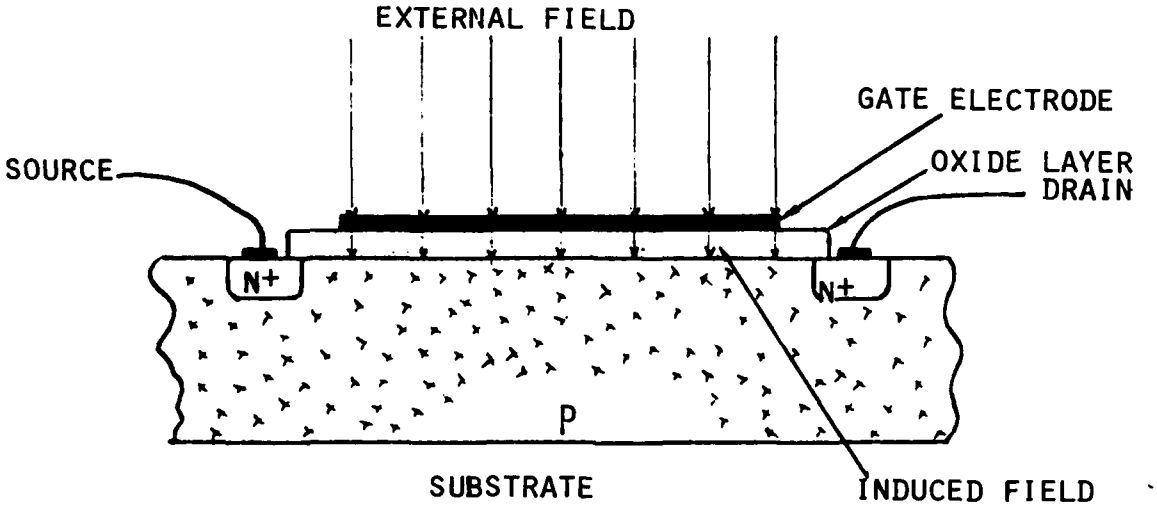


Figure 1.2 Schematic view of cross section of Floating Gate Field Effect Transistor. The gate metalization electrode which sits atop the oxide layer has no external electrical contact.

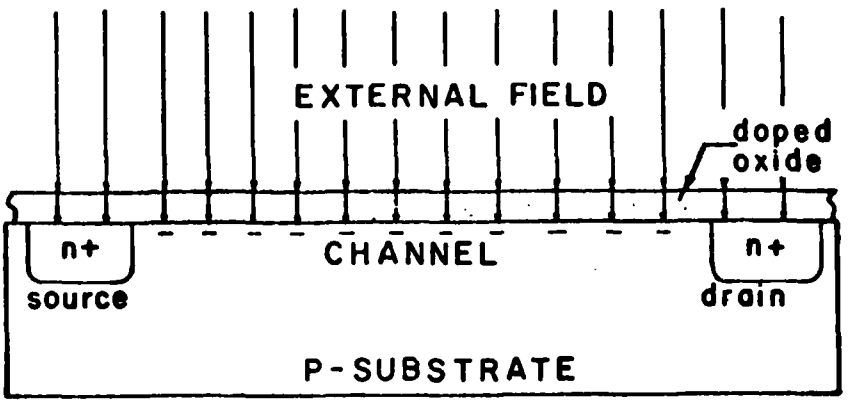


Figure 1.3 Schematic view of cross section of Direct Gate Field Effect Transistor. The gate metalization electrode is completely absent.

In the final phase of the research effort, both FGFET and DGFET devices were interfaced to a synchronous detection system to create a working dc field measurement instrument.

The sections that follow will describe in detail each phase of the research effort.

1.3 Description of Laboratory Facilities

All experiments, with the exception of the probe testing in vacuum reported in Section 7, were performed in the High Voltage Laboratory at Boston University. The experiments of Section 7 were performed in the vacuum chamber at the Air Force Geophysics Laboratory, Hanscom Air Force Base, MA. High voltage testing was performed inside a specially constructed test cage shown in Figure 1.4. Included in the test cage were a 0-40 kV Universal Voltronics power supply module, with appropriate safety interlock equipment. The high voltage cage was also equipped with a calibrated digital readout to facilitate accurate measurements of applied high voltage.

Electronic circuit development and testing was facilitated by the use of a Tektronix Model 5000 series instrument rack and Model 2215 oscilloscope, both of which were specifically purchased for use in the research project. Other instruments used in the project, but already available at Boston University, included various digital volt meters, signal generators, a Hewlett Packard oscilloscope camera, and a Heath model ET3400 microprocessor controller. These instruments, and their locations on an instrument rack organized for use in the project are shown in the Figure 1.5.

Figure 1.4 Photograph of High Voltage Test Cage

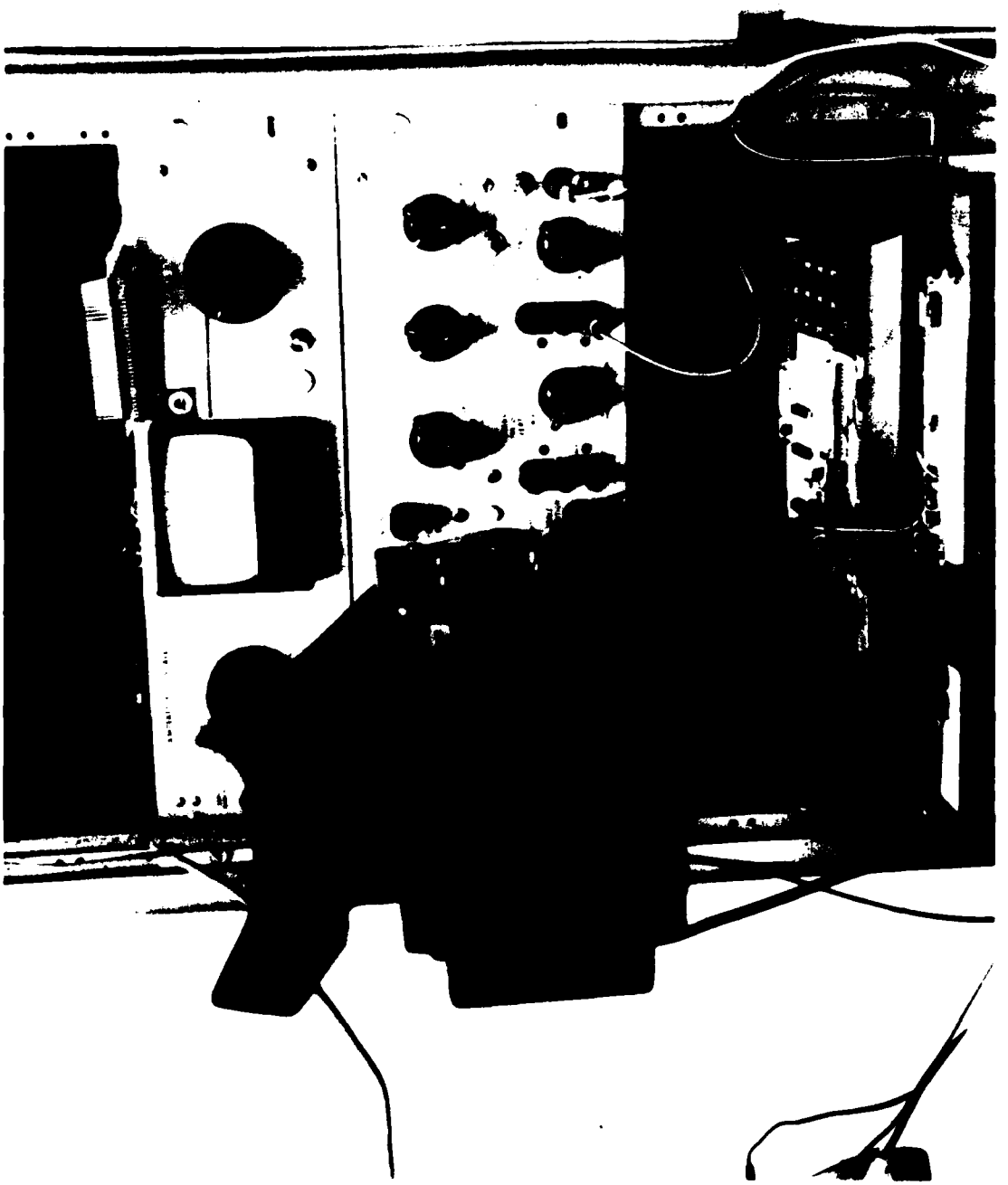


Figure 1.5 Instrument rack used to supplement the test cage

The testing of component circuitry in various temperature cycles was accomplished with the use of a model SK2101 thermal test chamber made by Associated Testing Laboratories. Temperature cycles in the range 25°C - 75°C were routinely obtained for the testing of various circuits used in the design of the probe heads described in Section 6.

The fabrication of the Floating Gate Field Effect Transistor, described in Section 4, was accomplished with the aid of a Hensoldt-Wetzlar 40X power binocular microscope and an assortment of dental exploring tools, obtained from a local supply house. The microscope was obtained from the Department of Biomedical Engineering at Boston University, as was the micromanipulator used in the fabrication experiments described in Section 6.

Often in the course of the research experiments, it was neccessary to record the output of a sensor over a long period of time. Because the sweep speed of the oscilloscope limited its time resolution to at most a minute or so, a method was required for obtaining extended sweep times for the various sensor signals. Extended time records of various sensor signals were thus obtained using an oscilloscope and Hewlett Packard oscilloscope camera coupled to the Heath ET3400 microprocessor controller. The controller was used, with the aid of a digital to analog (D/A) converter, to drive the horizontal sweep of the oscilloscope at a very slow rate. At each digital increment of the controller, the electronic shutter of the camera was also activated, so that the oscilloscope was in effect operated as a very slow sweep chart recorder. In this manner, time records of

sensor signals could be obtained over periods of minutes, hours, or even days. (In one case a block of data was obtained over a period of twelve days).

All machining and fabrication tasks, with the exception of the Direct Gate Field Effect Transistor, were performed either in the High Voltage Laboratory, or in the College of Engineering Machine Shop at Boston University.

Other photographs of the experimental facilities, and of the finished surface potential probe described in Section 6, are included in Figures 1.6 through Figure 1.8

Figure 1.6 High voltage cage, with ac driver (top left), synchronous detector box (top right), light shielding foil in place. DGFET probe is in foreground.

Figure 1.7 Closeup view of FGFET probe head.

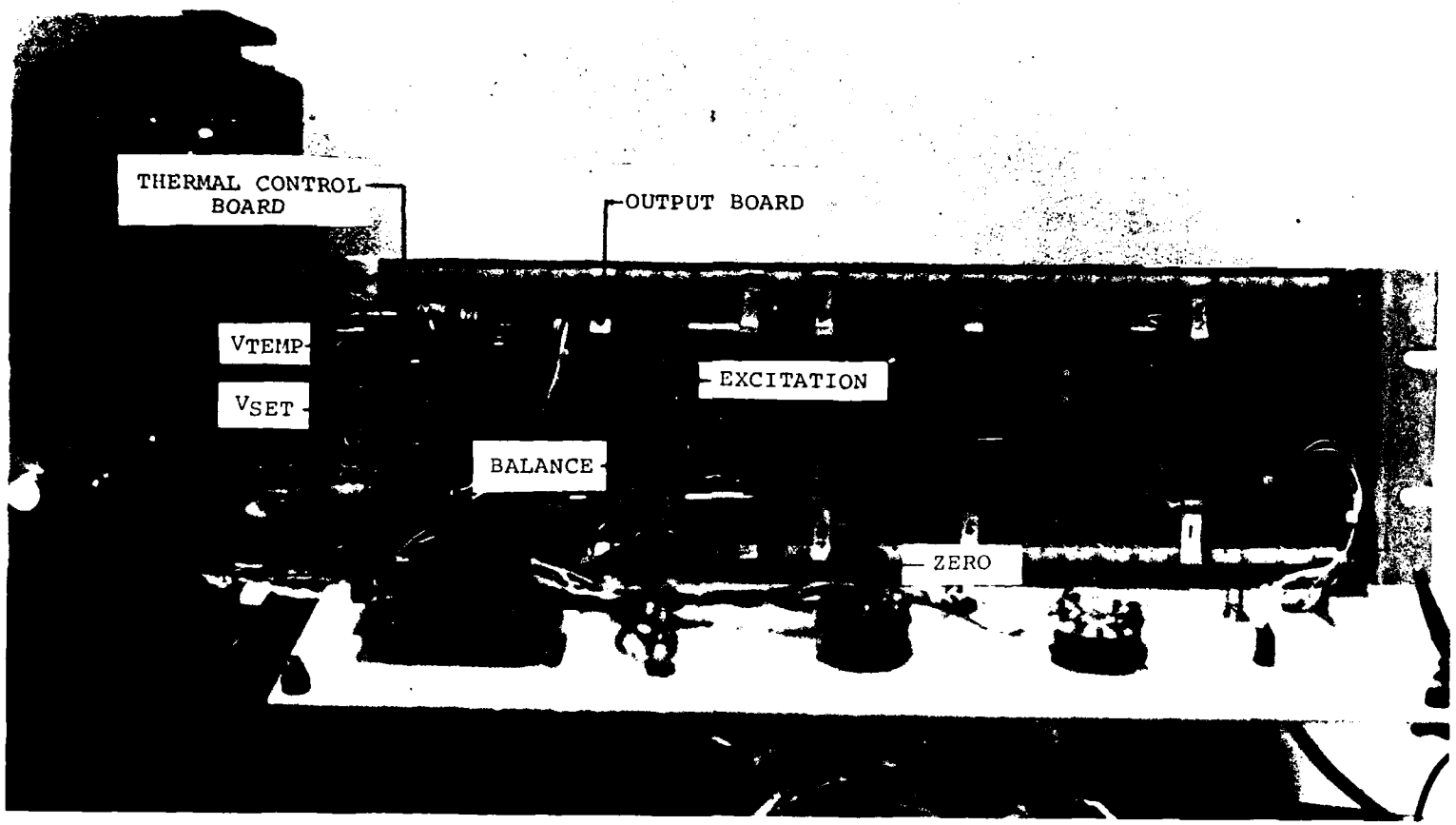


Figure 1.8 Inside of synchronous detector box.

2. TESTS ON UNMODIFIED MOSFETS

In the initial stages of the research, tests were performed on unmodified "off the shelf" metal oxide semiconductor field effect transistors (MOSFET'S), in an effort to gain insight into the general properties of the devices, and to assess the feasibility of the devices for use in the measurement of electrostatic potentials and fields. The Motorola 2N3797 and the RCA 3N138 transistors were selected for tests, because they were the devices most easily obtained from local suppliers.

Both of these devices belong to the depletion mode family of FET's, which have the property that a finite drain current can flow in response to V_{DS} when the gate to source voltage V_{GS} is zero. By contrast, simple enhancement mode MOSFET'S require the gate voltage to be above a threshold value on the order of a few volts, before drain to source conduction can occur. The internal "biasing" of the gate voltage above this threshold level in the depletion mode MOSFET is accomplished by implanting into the oxide layer, which insulates the gate from the substrate, a layer of fixed bound charge, usually referred to as the oxide layer charge Q_{SS}. A depletion mode device, with its internal biasing, is required if the MOSFET is to be used to measure fields, because the gate voltages induced in response to practical electrostatic fields and potentials are exceedingly small in magnitude - usually several orders of magnitude below the enhancement mode threshold level of V_{GS}. At the same time, a depletion mode device allows <u>both</u> positive and negative surface potentials to be measured, by allowing both positive and negative

incremental induced voltages, above and below the biased gate voltage, to occur.

The capacitively coupled external electrode structure shown in detail in Fig 2.1 was used to test the response of the devices to an externally applied electric field. The sampling electrode, though insulated from the lower grounded plate, appears at capacitive quasi-ground potential via its connection to the FET gate, while the upper plate, which is connected to a high voltage supply, imposes a uniform electric field on the lower plate. The electric field thus capacitively induces a voltage on the gate of the MOSFET in response to the turn-on transient of the high voltage supply. The equivalent circuit that represents the configuration of Figure 2.1 is shown in Figure 2.2, which suggests that the voltage induced on the gate of the MOSFET is given by:

$$V_{GS} = V_o \frac{C_o}{C_{GS}+C_o} = E_o \frac{\epsilon_o A}{C_{GS}+C_o} \qquad (2.1)$$

where C_{GS} is the gate to substrate capacitance, C_o is the capacitance appearing between the sampling segment and the source of field E_o, and A is the area of the sampling segment.

In the laboratory experiments, the drain and source leads were excited by the circuit of Figure 2.3. Note in this circuit that a second reference FET, which is not exposed to the external field, is used to track the operating point of the sensing FET. If the devices are well matched, then the gate voltage on the reference transistor will equal the induced gate voltage on the sensing transistor.

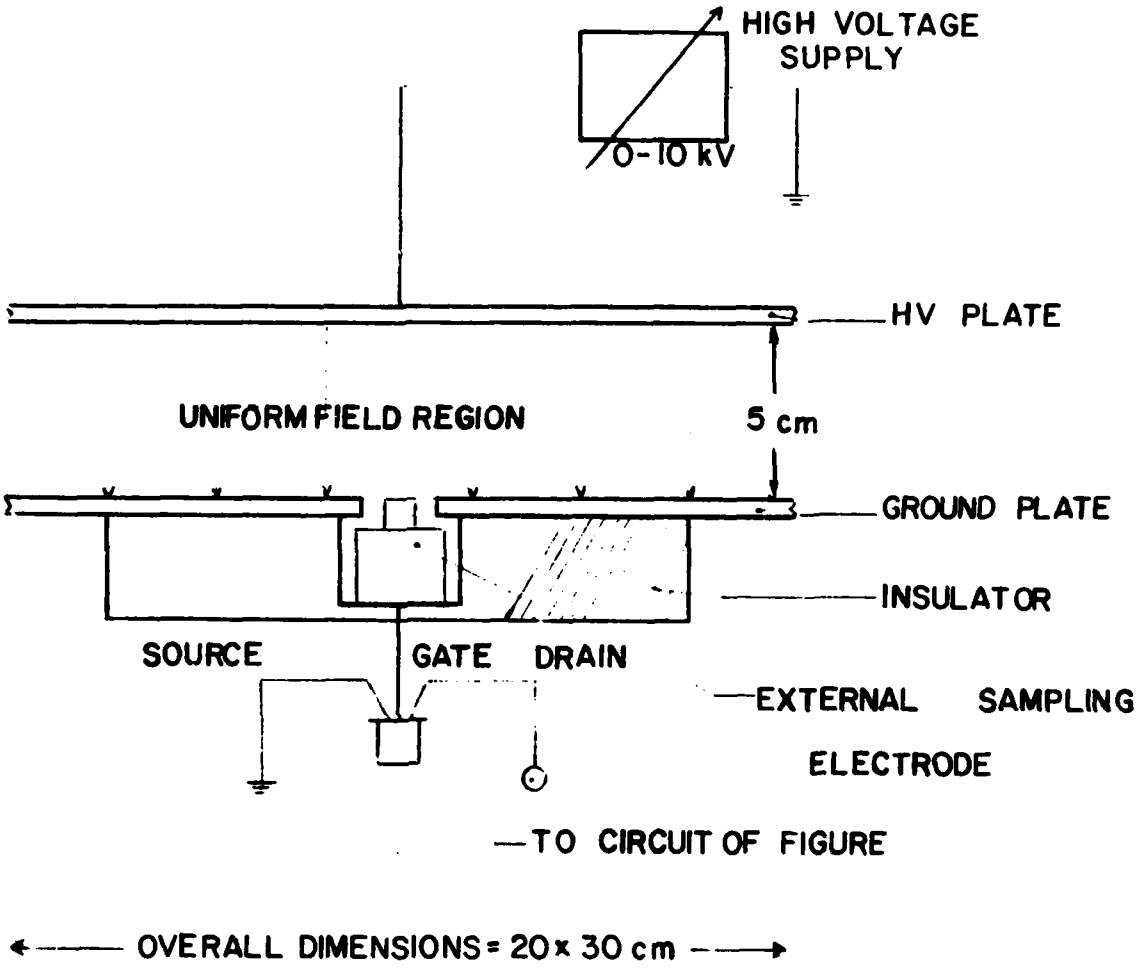
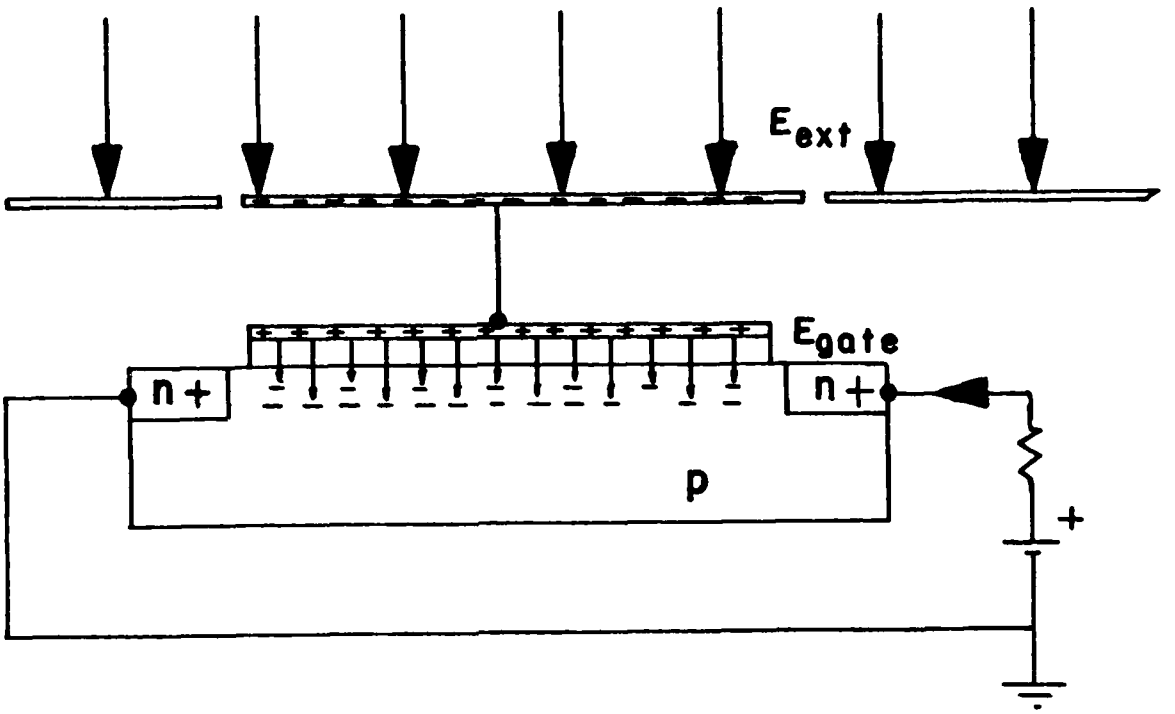
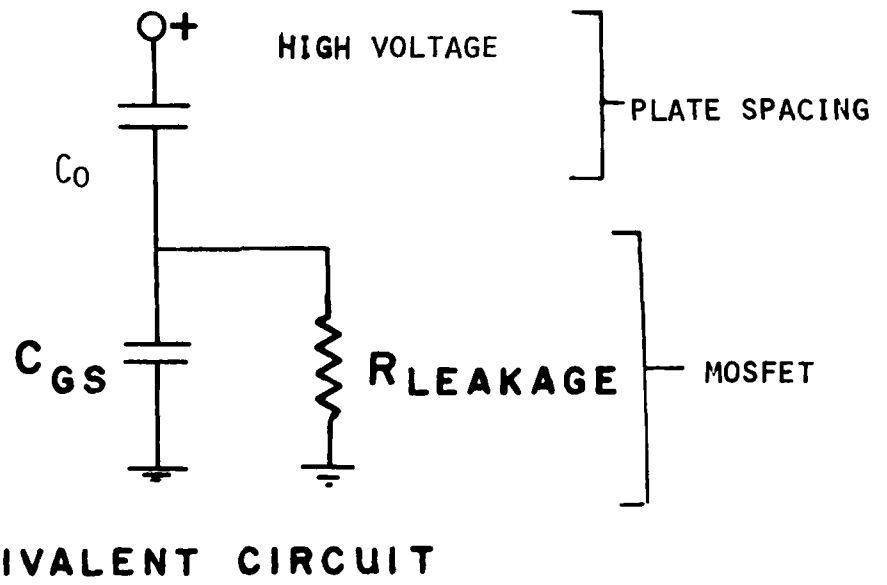


Figure 2.1 Detailed view of electrode structure used to test unmodified MOSFET devices.





EQUIVALENT CIRCUIT

Figure 2.2 Equivalent circuit of capacitively coupled MOSFET field sensor. The external field is represented by V_o and C_o.

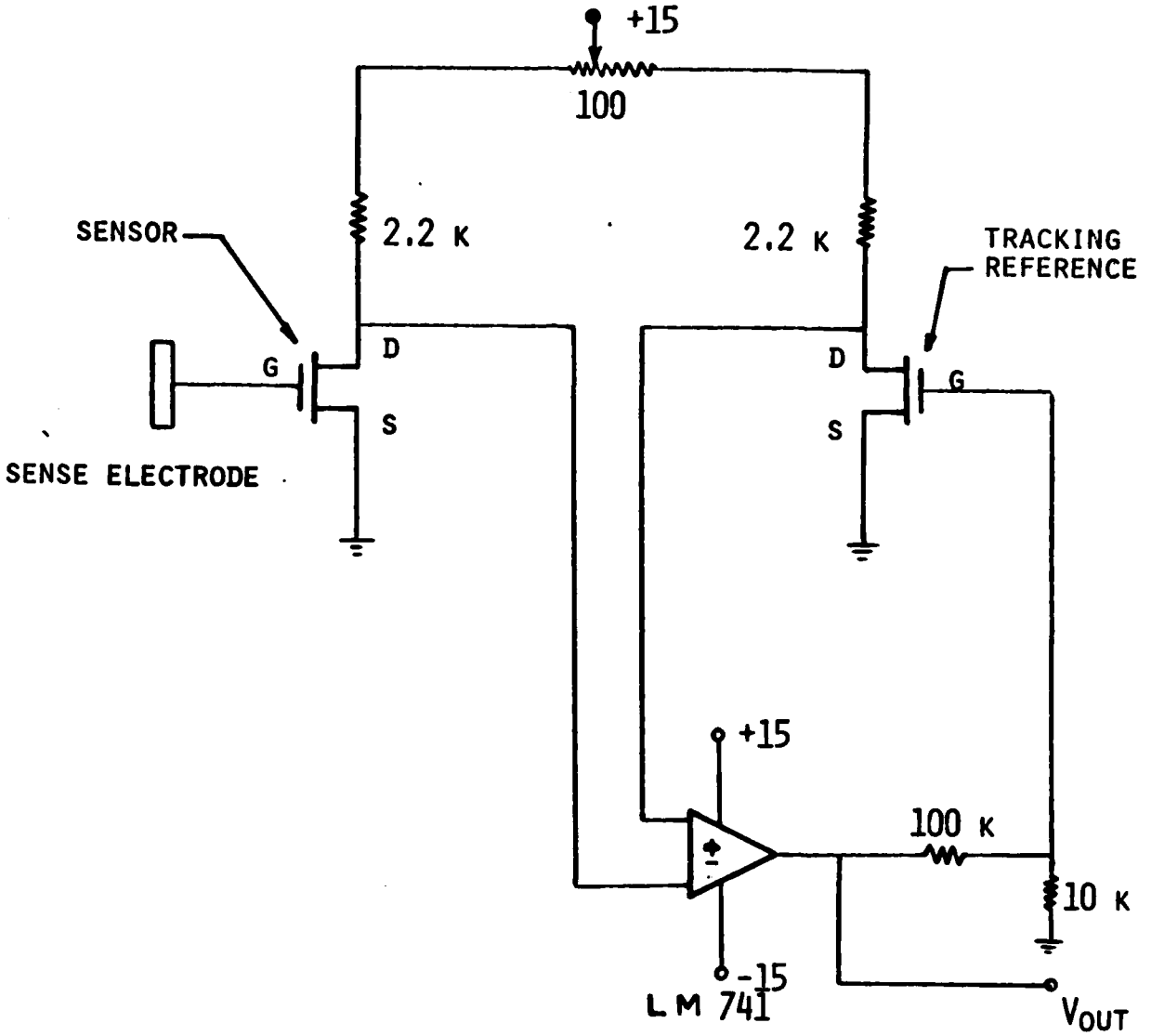


Figure 2.3 Circuit used to excite sensor and reference in unmodified MOSFET tests.

A plot of the output of the circuit of Figure 2.3, versus applied high voltage, is shown in Figure 2.4. As expected, the output is a linear function of the input. The magnitude of output voltage observed in the experiments is also of the proper order of magnitude suggested by equation 2.1. Note that in obtaining the plot of Figure 2.4, the sensor electrode was discharged before each reading, and the readings were obtained quickly - within several seconds of field energization.

While this system is capable of measuring external fields, the readings produced by it when the field is first turned on are not held indefinitely. Rather, they are seen to decay in time, with a time constant on the order of ten or fifteen minutes, or at most one hour. The mechanism for this decay is RC relaxation of the voltage induced on the gate capacitance through leakage resistance paths that shunt the gate electrode to the source, drain, and substrate of the transistor. These leakage paths appear across the header package of the MOSFET itself, over the surface of the oxide layer, and through the bulk of the oxide layer. Given a gate to substrate capacitance C_{GS} of about 100 pF, the resistance of the total leakage path is seen to be on the order of 10^{13} ohms.

Although the sensing system described in this section is far from optimal for use on space vehicles, the experiments do show that the MOSFET structure is capable of measuring electrostatic fields. These experiments also motivated development of both the Floating Gate Field Effect Transistor (FGFET) and Direct Gate Field Effect Transistor (DGFET), which were both investigated as improved alternatives to the unmodified MOSFET field sensor.

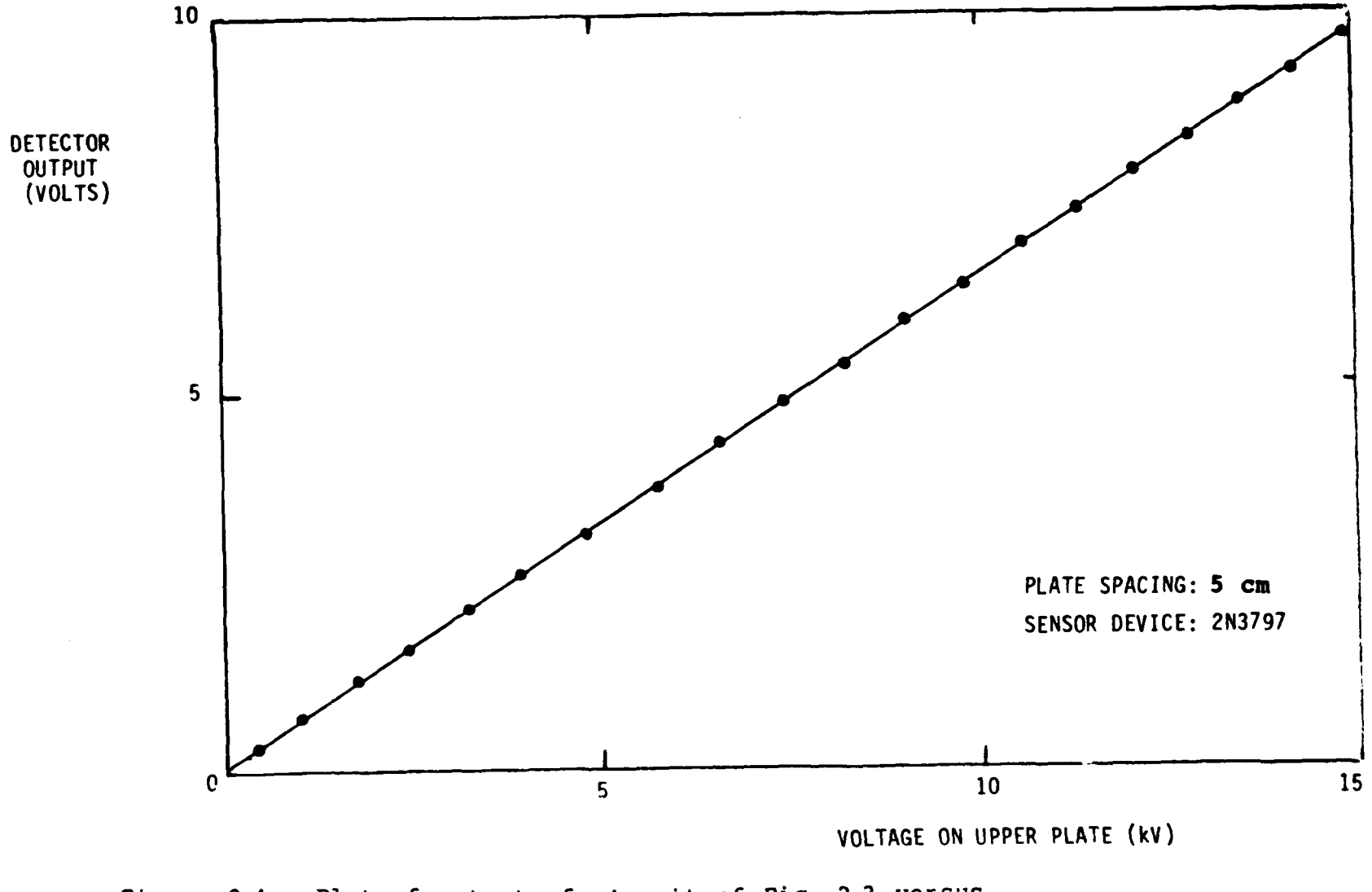


Figure 2.4 Plot of output of circuit of Fig. 2.3 versus voltage applied to upper plate. Plate spacing was 5 cm.

3. DEVELOPMENT OF THE FLOATING GATE FIELD EFFECT TRANSISTOR

3.1 FGFET Fabrication Method

During the course of the research activities, two types of commercially available depletion mode MOSFET transistors were successfully transformed into working FGFET devices. Both the RCA 3N138, and the Motorola 2N3797, which are available in metal TO-18 packages, were subjected to the following now standardized fabrication procedure. Modification begins with the removal of the metal cover from the package header, whose dimensions are shown in Fig 3.1. The diameter of the TO-18 transistor case permits its being mounted in a 3/16" machine collet so that the entire transistor package can be rotated. With the case rotating at slow to moderate speed in a milling machine or lathe, a sharp "Xacto" razor knife is held, by hand, against the side of the case, about 1/32" above the rim of the transistor, as shown in Figure 3.2. With moderate pressure, the case can be severed evenly in a few minutes, leaving the bare package header, with exposed FET chip, free to fall away from the case shell. The shell can be saved for later use as a removable protective cover for the sensor device. (Note that in this machining step, as well as in the lead severing step to follow, the MOSFET gate is still externally connected, and care should be exercised to avoid ESD burnout.)

Next, with the header mounted beneath a 40X power binocular microscope, the gate lead severing operation is performed. A needle-point dental exploring tool (or ordinary stainless steel

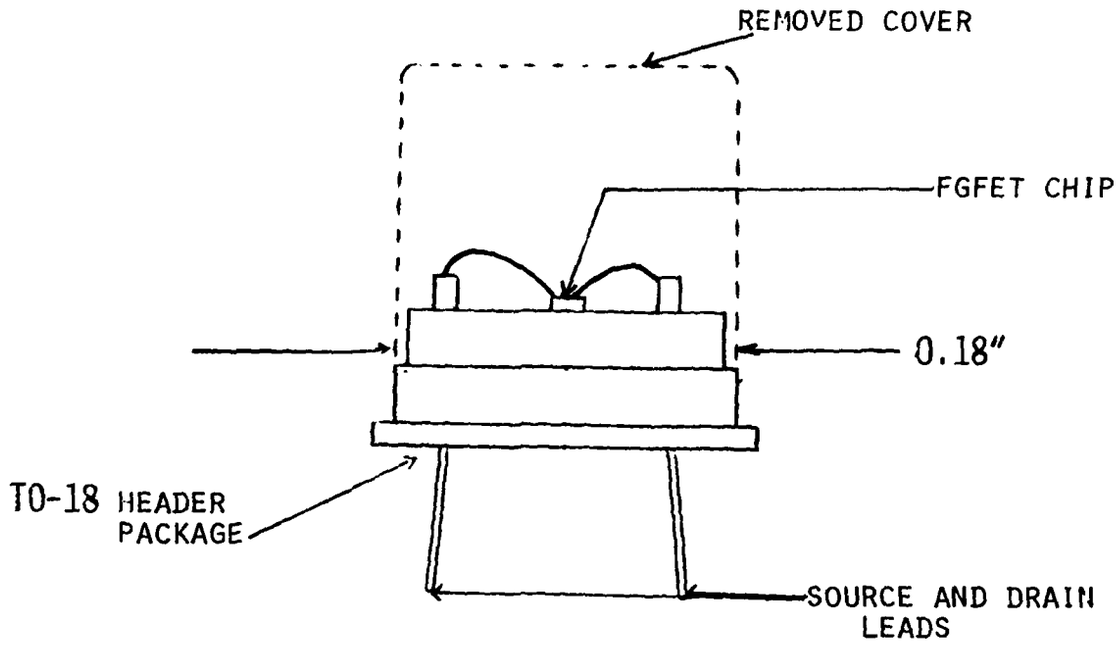


Figure 3.1 Dimensions of the TO-18 metal case transistor package.

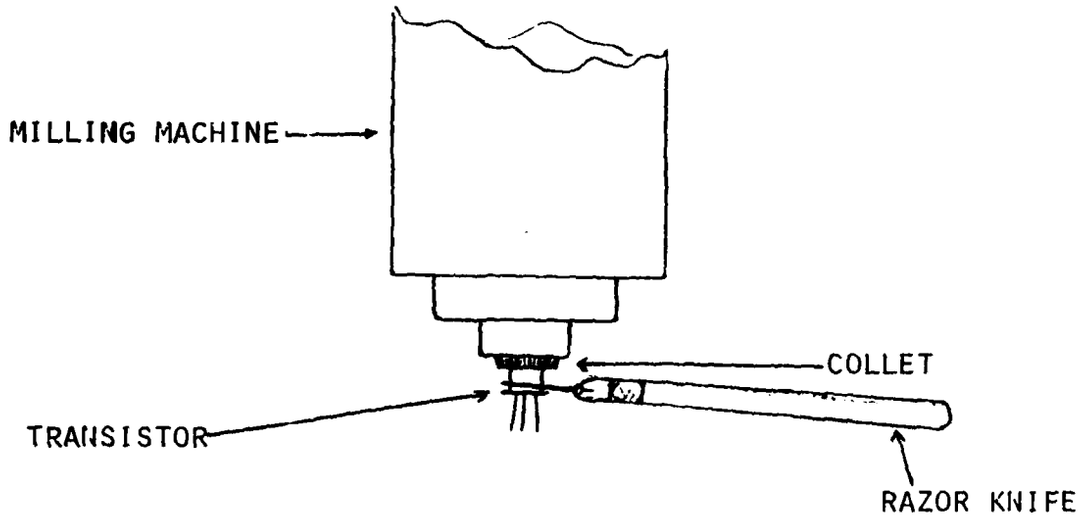


Figure 3.2 Method of cutting open transistor case. With the case held in a rotating milling machine or lathe collet. a razor knife is used to cut open and separate the outer case cover.

sewing needle) is placed beneath the bonding wire just adjacent to its point of contact with the gate pad. Lifting the needle tip breaks the bond wire at its weakest point, i.e. the place where it is spot welded to the gate pad. The remaining piece of bond wire, now dangling from the header pin, is broken off by working it back and forth several times until breakoff occurs at the header pin. After this bond wire operation, the gate of the FGFET is left isolated and electrically floating.

Top views of both the 2N3797 and 3N138 devices, showing the metalization layouts, and locations of the gate, source, and drain pads (to which the bonding wires are connected) are shown in Figs. 3.3 and 3.4.

3.2 Experimental Observations of FGFET I-V Characteristics

In this section, the peculiarities of the FGFET I-V characteristics, as first observed in the laboratory, will be discussed. Attempts to explain the features of the I-V characteristics leads to a simple model for the device, which also describes its behavior when exposed to an electric field. This model will be discussed in Section 3.3.

The I-V characteristic curves of one particular unmodified MOSFET device, as measured on a Tektronix curve tracer, are shown in Figure 3.5. The I-V characteristics of the same device after FGFET modification are shown in Figure 3.6. Contrary to one's intuition or expectations, the FGFET curve does not look like any single MOSFET curve of constant V_{GS}. Rather, if the curves of Figure 3.5 and 3.6 are interpreted as coming from the same physical

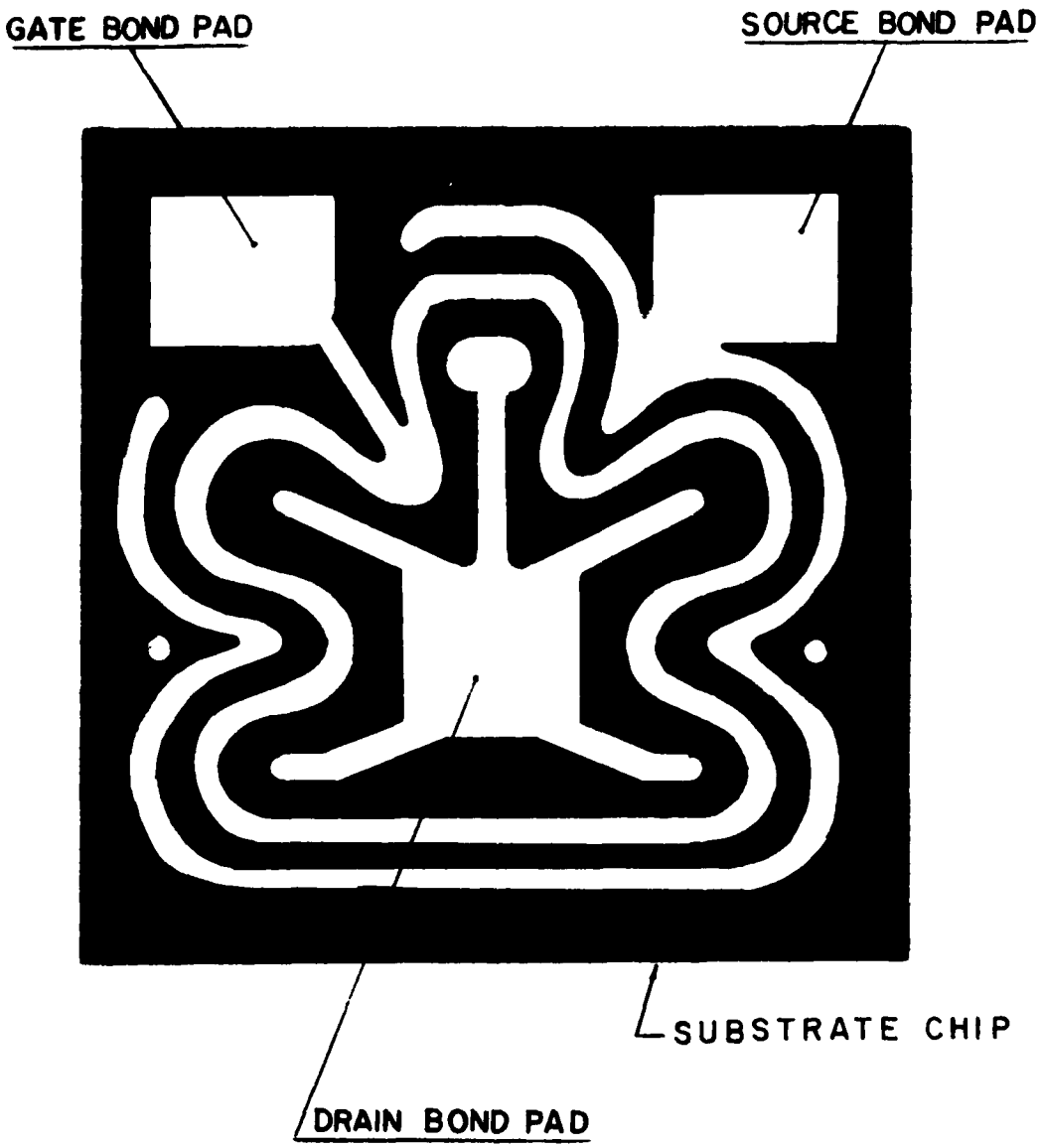


Figure 3.3 Metalization layout for the 2N3797 MOSFET transistors.

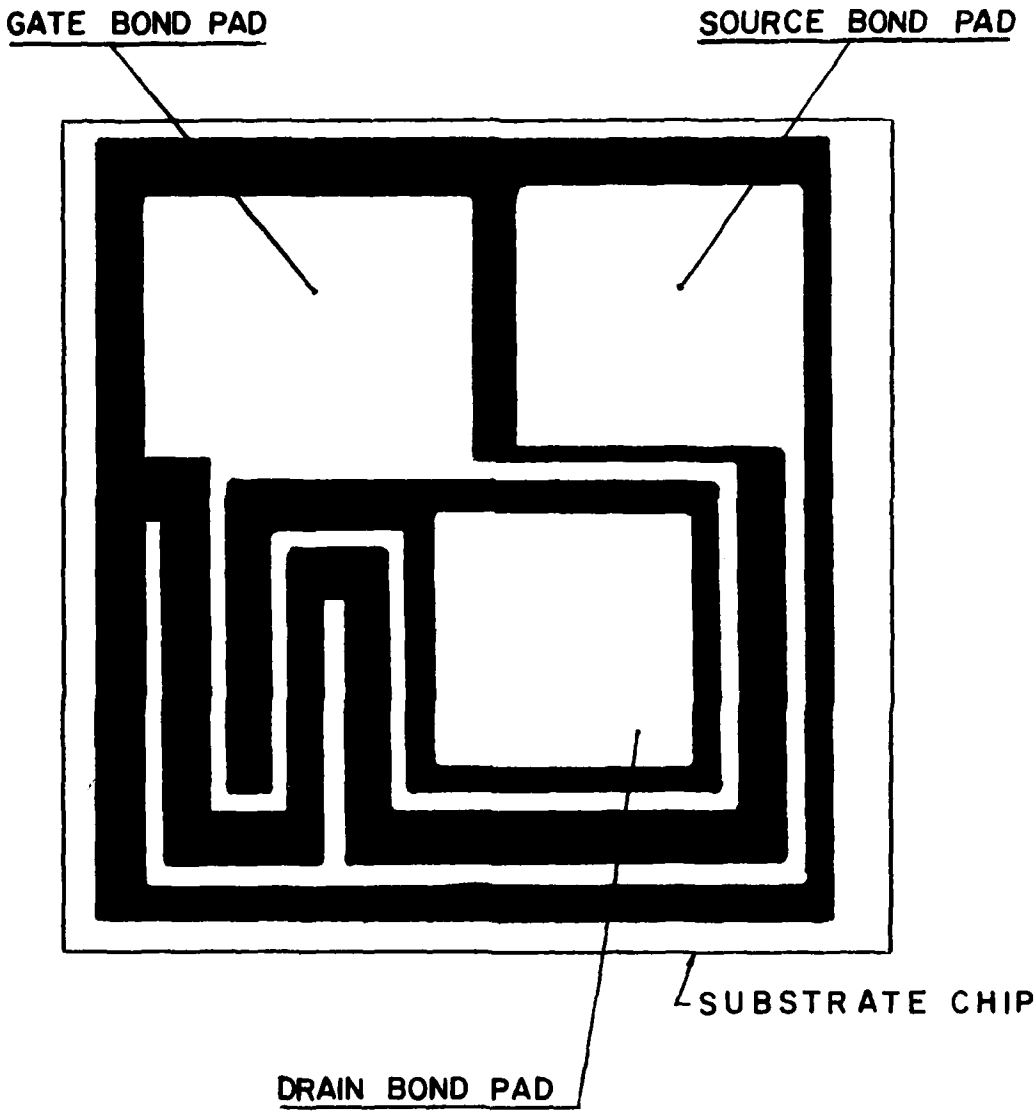


Figure 3.4 Metalization layout for the 3N138 MOSFET transistors.

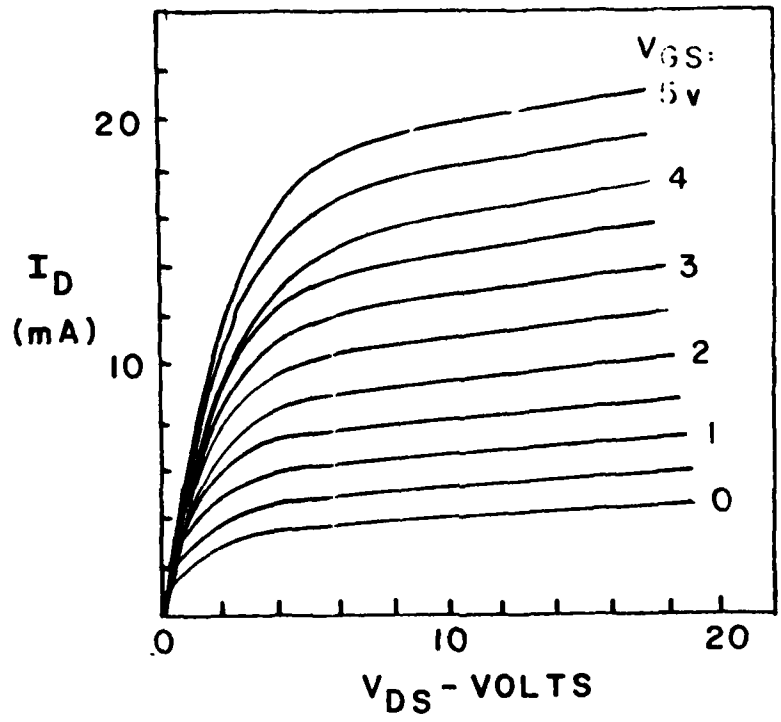


Figure 3.5 I-V characteristic curves of unmodified 2N3797 MOSFET.

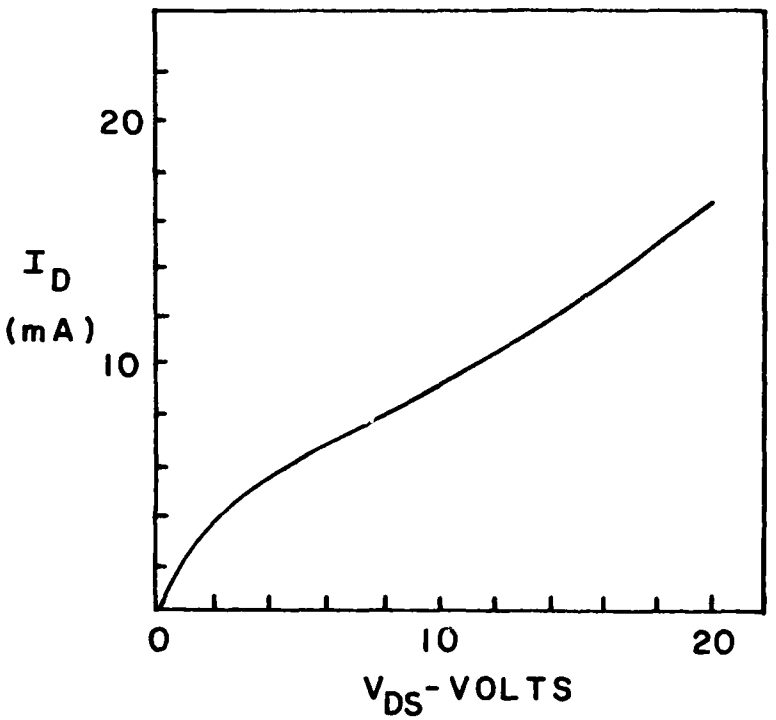


Figure 3.6 Single I-V characteristic curve of the 2N3797 MOSFET of Fig. 3.5 after FGFET modification.

device, the instantaneous value of V_{GS} on the FGFET is seen to increase with increasing values of drain to source voltage V_{DS}.

If the device is left in the curve tracer for any appreciable length of time, another interesting effect is observed. The I-V curve is seen to gradually move downward, as seen in Figure 3.7, which shows the position of I-V curve of the FGFET of Figure 3.6 at forty minute intervals.

These two interesting features of the FGFET I-V characteristic will be explained by the theoretical model of the next section. This theoretical model is useful because it also predicts the transient response of the sensor when an external electric field is applied.

3.3 Theoretical Model for the FGFET Device

The phenomena described in the previous section can be explained by utilizing a simple, passive, distributed RC model for gate coupling in the device. The motivation for modeling the FGFET gate-to-substrate coupling as a passive RC network comes from an examination of the structure of the device, shown schematically in Figure 3.8. The gate electrode, which sits atop the oxide layer covering the silicon substrate, is for all practical purposes insulated from the substrate. When long term dc exitation of the gate is considered, however, both the bulk and surface resistance of the oxide layer must be taken into account. Because the gate is in close proximity to the drain and source contact pads, it is also capacitively coupled to both. A

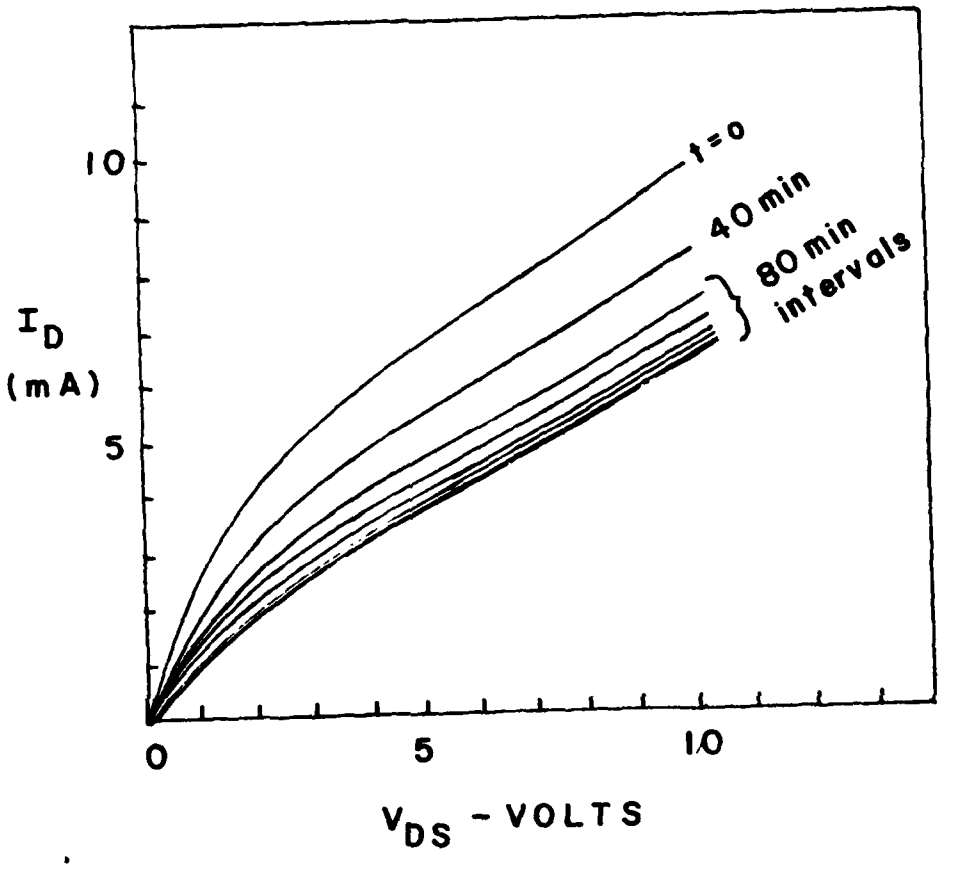


Figure 3.7 Change with time of position of 2N3797 FGFET curve as seen on curve tracer as dc component of V_{DS} excitation decays to equilibrium.

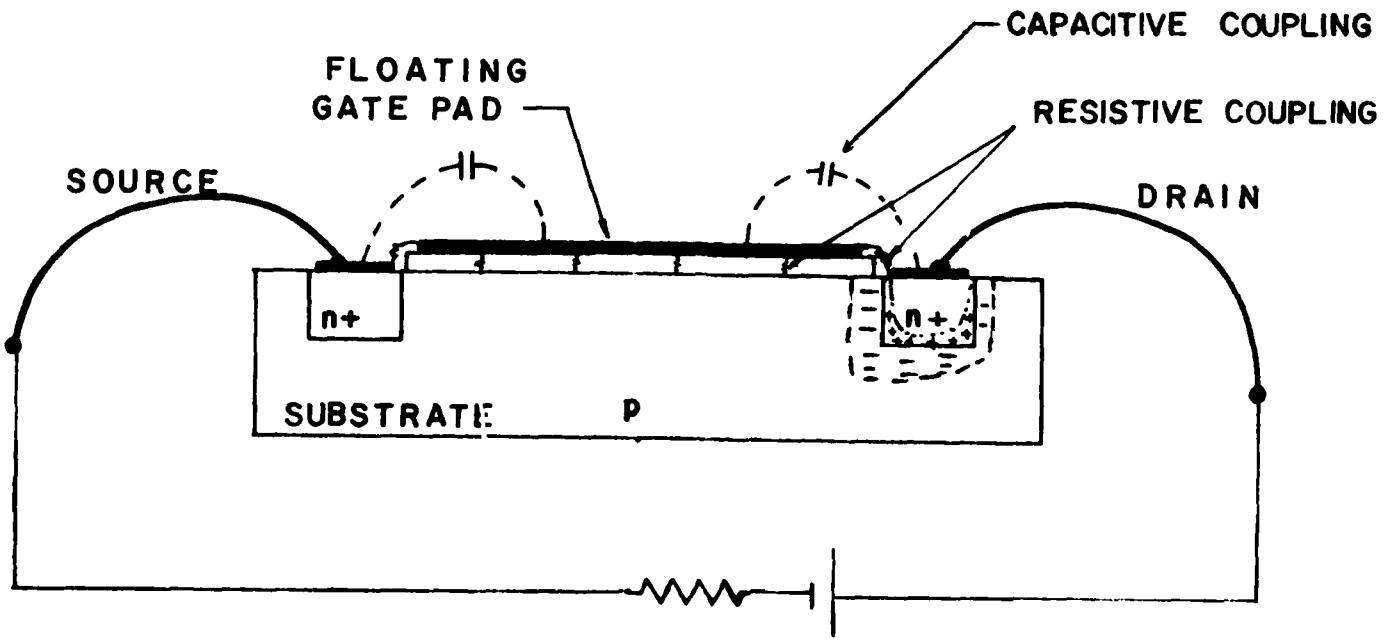


Figure 3-8 Schematic diagram of cross section of typical FGFET device, showing capacitive coupling between drain, source, and gate electrode.

simple model for the FGFET thus follows in which the gate pad is both capacitively and resistively coupled to the drain and source leads by a simple lumped RC network, as shown in Figure 3.9. Even without detailed analysis, this RC model for the FGFET can explain the anomalies of the I-V characterisitc curve described in Section 3.2. The general shape of the I-V characterisic, for example, can be explained by noting that the curve tracer excites the value of V_{DS} with an essentially ac waveform. A gate voltage will thus be induced by the capacitive divider that is midway between the positive drain voltage and the grounded source lead. By overlaying the traces of the device before and after FGFET modification, (Figures 3.5 and 3.6), a plot of this induced V_{GS} versus applied V_{DS}, in the domain where the capacitive coupling to the gate dominates, can be made. Such a plot is shown in Figure 3.10, which indicates that the ratio of V_{GS} to V_{DS} is indeed a constant, and is equal, for this particular device, to about 0.2. In general, this ratio will depend on the exact details of device geometry and layout. Note that in the particular plot of Figure 3.10, the curve does not cross through the origin, indicating that when the measurements were made, a small random dc static charge was left on the gate by some prior mechanism, leading an apparent dc offset value for V_{GS}.

The same RC model for the FGFET can explain, at least to first order, the change in the I-V curve with time, indicated in Figure 3.7. Although the capacitive coupling between gate, drain, and source will dominate when the excitation to the device is an ac voltage, the resistive coupling between gate and substrate

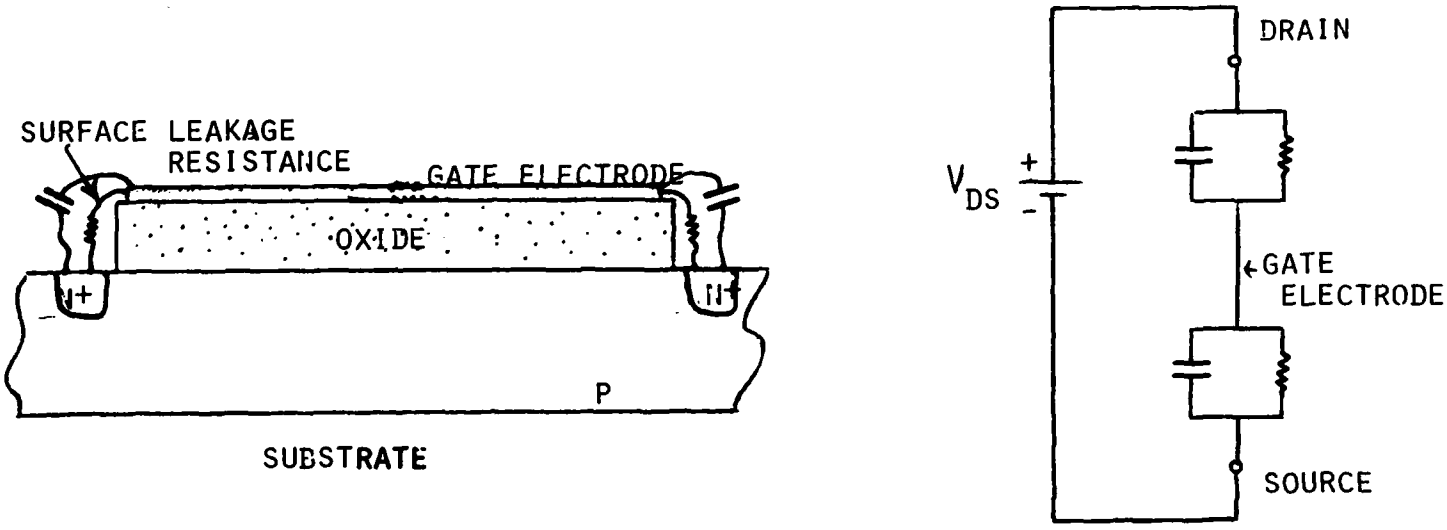


Figure 3.9 Simple lumped element model for FGFET gate coupling.

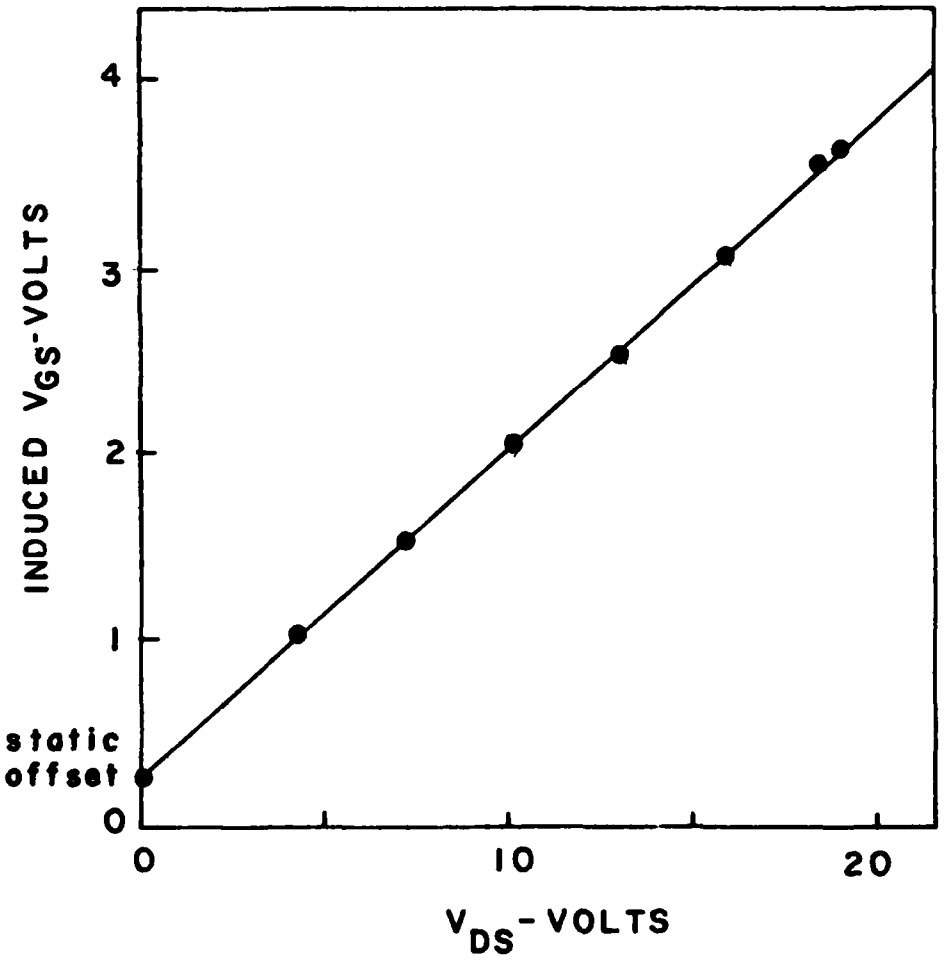


Figure 3.10 Plot of induced V_{GS} versus applied V_{DS}, in the domain where capacitive coupling dominated. Ratio is about 0.2.

will eventually respond to any dc component of device exitation. Because the curve tracer excites the FET only into the first quadrant, a net dc component is consiscantly applied to the device. The corresponding dc component of induced gate voltage will thus gradually relax from the initial capacitively determined value to a value determined by the resistive coupling between gate and substrate. Even without knowledge of the details of this coupling, it should be evident that the transient will be exponential in time, if the simple RC model is valid. The transient can indeed be shown to be exponential in time by examining the information provided by Figure 3.10.

In making the plot of Figure 3.10, the values of V_{GS} induced in response to the instantaneous value of V_{DS} applied by the curve tracer, were determined. Figure 3.11 shows a semi-logarithmic plot vs time of these values, which, because it is a straight line, indicates that the induced gate voltage indeed follows an exponential transition in time from its initial to its equilibrium value, with a time constant equal to about 160 minutes. For a typical gate-to-substrate total capacitance of about 100 pF, the oxide layer resistance is seen to be on the order of about 10^{14} Ohms.

This simple RC coupled model for the FGFET makes it possible to predict its static i_D-V_{DS} curve. The "static", or "equilibrium", curve describes the behavior of the FGFET when the resistive, rather than the capacitive, coupling to the gate dominates, i.e. when the energized device is allowed to come to static equilibrium after many time constants.

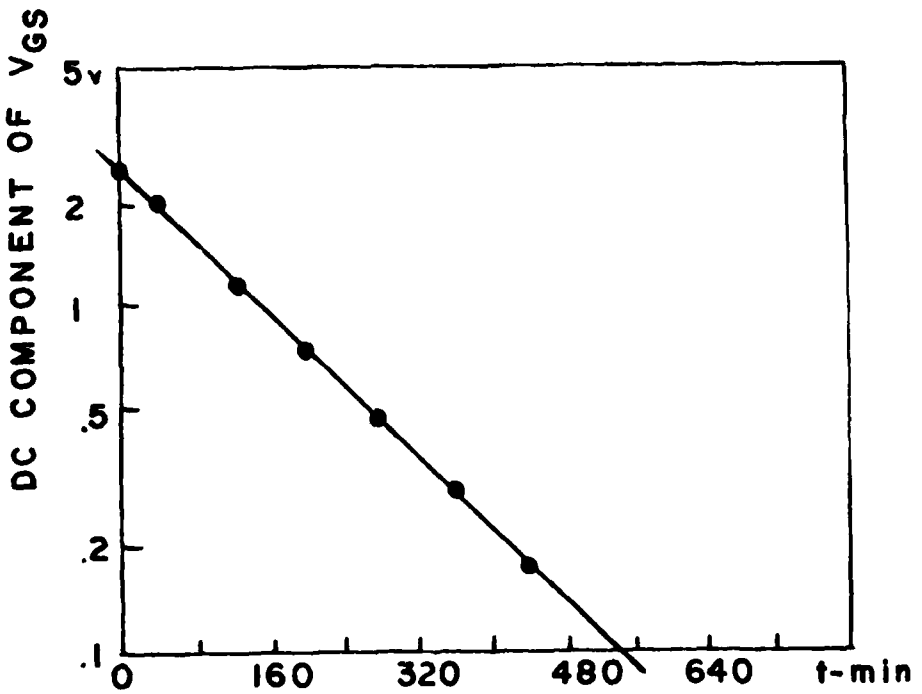


Figure 3.11 Decay versus time of peak value of induced V_{GS}, occurring at peak value of V_{DS} applied by the curve tracer.

Although the resistive coupling between gate and substrate can be tr eated as a simple lumped element circuit, it is really distributed, and thus must be analyzed as a continuum before appropriate values can be assigned for lumped element of Figure 3.9. Such a continuum model is shown in Figure 3.12 where a uniform resistivity oxide layer electrically connects gate electrode to each point on the substrate surface. This model presumes that the volume resistance of the oxide layer is more significant than the surface resistance at its edges - an assumption that can be relaxed later. The value of V_{GS} resulting from the simplified model is thus given by:

$$V_{GS} = \frac{1}{L} \int_{y=0}^{y=L} V(y)\ dy \qquad (3.1)$$

where V(y) describes the drain to source voltage distribution along the substrate. extending the length of the channel from the source end (y=0) to the drain end (y=L).

With the assumption that the device will respond as a conventional MOSFET to the value of gate voltage, whether induced or applied. V(y) will in turn be a function of V_{GS}[3]:

$$V(y) = V_{GS} \left[1 - \sqrt{1-y/L} \right] \qquad (3.2)$$

$$\text{for } V_{GS} < V_{DS}$$

(Because the induced V_{GS} will always be less than V_{DS} in the FGFET, the domain $V_{GS} > V_{DS}$ is not included in the above equation for V(y)). The solution of these two simultaneous equations requires numerical computation. The details of this computation are described in detail in the Master's Thesis of Edmund Walsh,

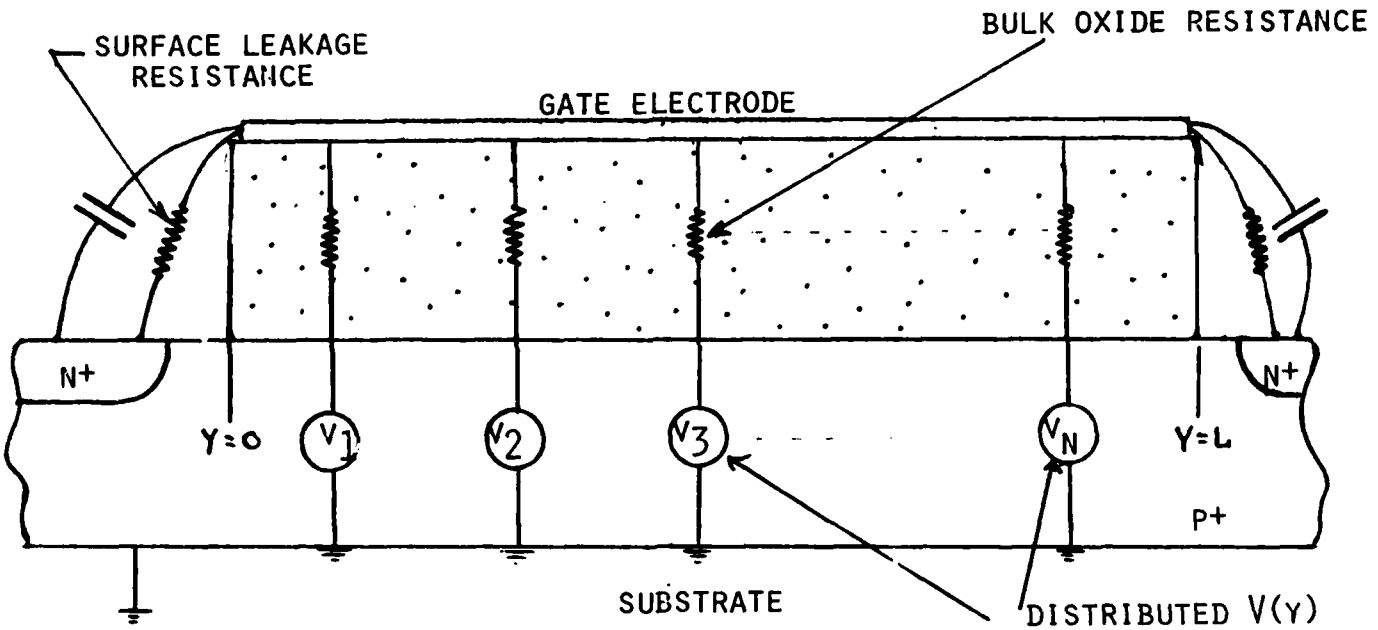


Figure 3.12 More detailed RC coupling model for FGFET. The gate electrode is coupled by lumped resistance and capacitance to the drain and source leads, and by distributed resistance to the voltage distribution V(y) along the channel length.

(included as Appendix D). The results of these computations yield the I_D-V_{DS} curve shown in Figure 3.13, which also includes data taken from a FGFET in the laboratory. The similarity between theory and experiment indicates that the RC coupled model for device behavior is a plausible one.

3.4 Response of FGFET to an Applied Electric Field

The ability of the FGFET to measure dc fields was evaluated with the same basic test configuration used for unmodified MOSFETS, except that the external sampling electrode was absent, as shown in Figure 3.14. The energized parallel plates provide a uniform field intensity in the region surrounding the device under test, which is embedded in the center of the bottom, grounded plate. With each FGFET biased by a fixed voltage V_{DS}, incremental changes in the drain current I_D were measured in response to the applied field. Figure 3.15 shows a plot of I_D versus field strength E_o for a typical device. From the value of I_D, and knowledge of the transconductance g_m (measured prior to FGFET modification), a value for the induced V_{GS} per unit field strength can be derived. A comparison of this experimentally realized gate voltage with the value predicted from the simple capacitive coupling model again shows good agreement between theory and data. Figure 3.16 shows a rough plot of I_D versus time for a fixed step of field energization. The sensor output decays with time, as expected from the simple RC gate coupling model given in Section 3.3. A comparison of the time constant for the decay of the field signal with the time constant for decay of the

dc self bias component shows both time constants to be about the same -- an expected result given that both phenomena are described by the same RC coupling model.

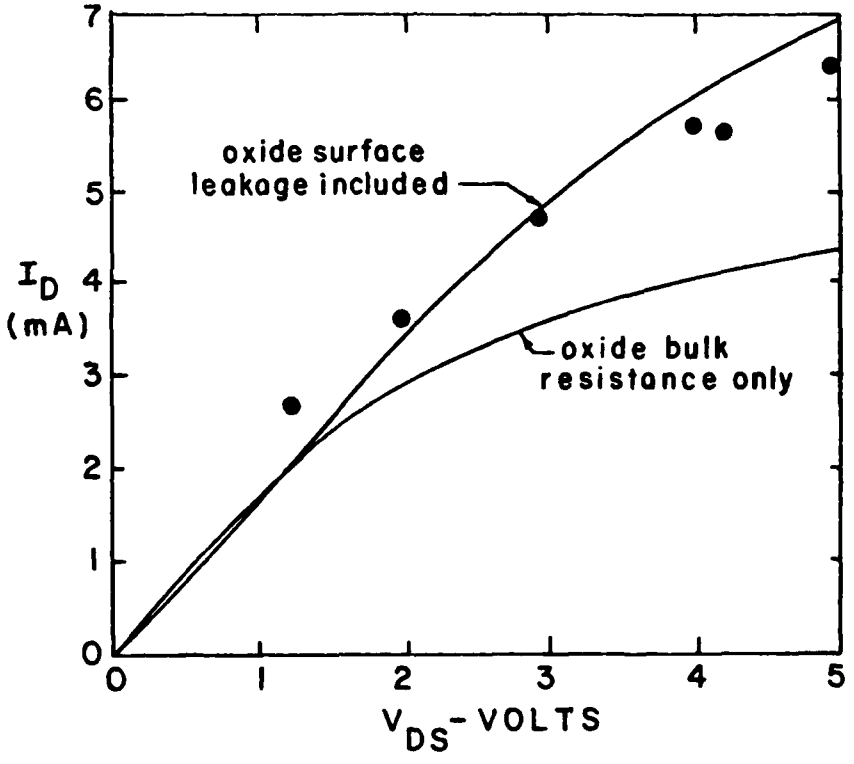


Figure 3.13 Numerically computed FGFET I-V curve using the distributed RC model of Fig. 3.12. Some data points taken on one FGFET device in static equilibrium (approx 16-20 hours between i_D-v_{DS} data points) are included for comparison. Similarity in shape between theory and experiment is evident.

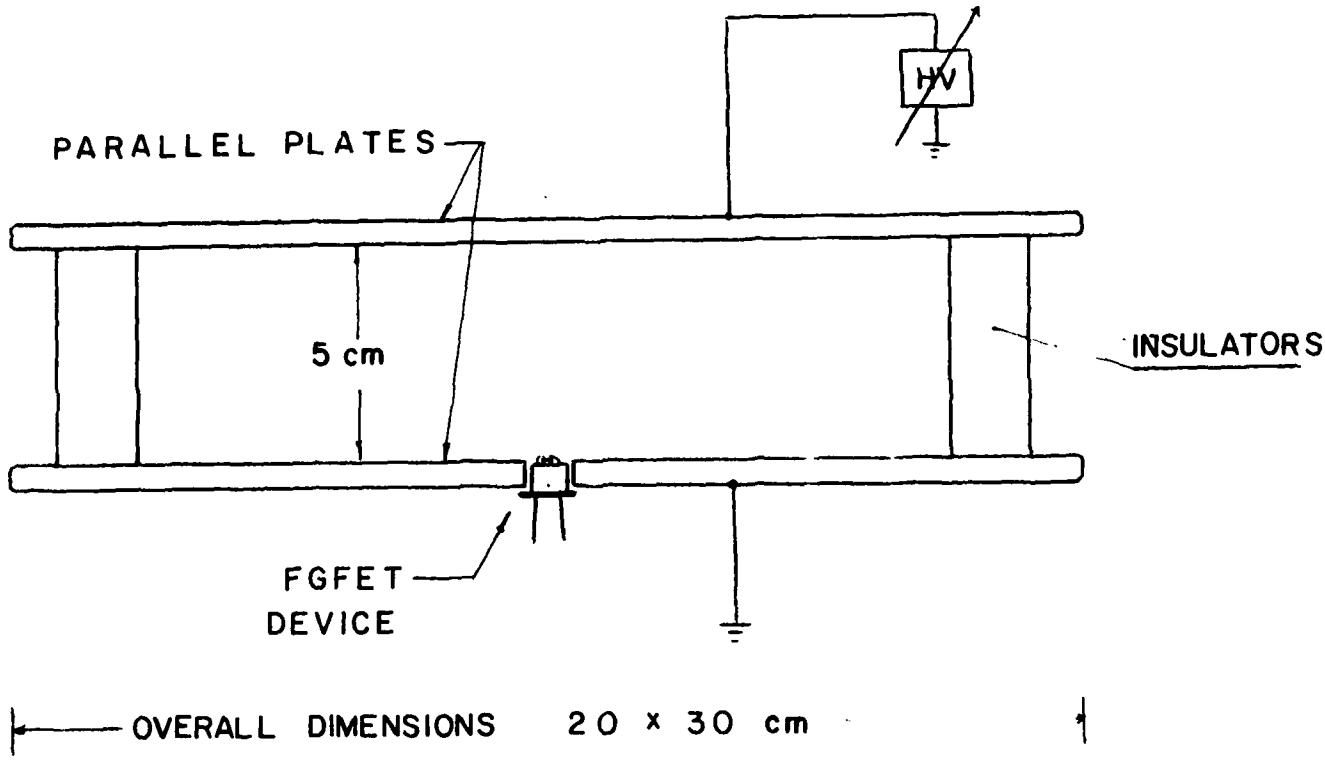


Figure 3.14 Electrode configuration used to test response of FGFET and DGFET to electric fields.

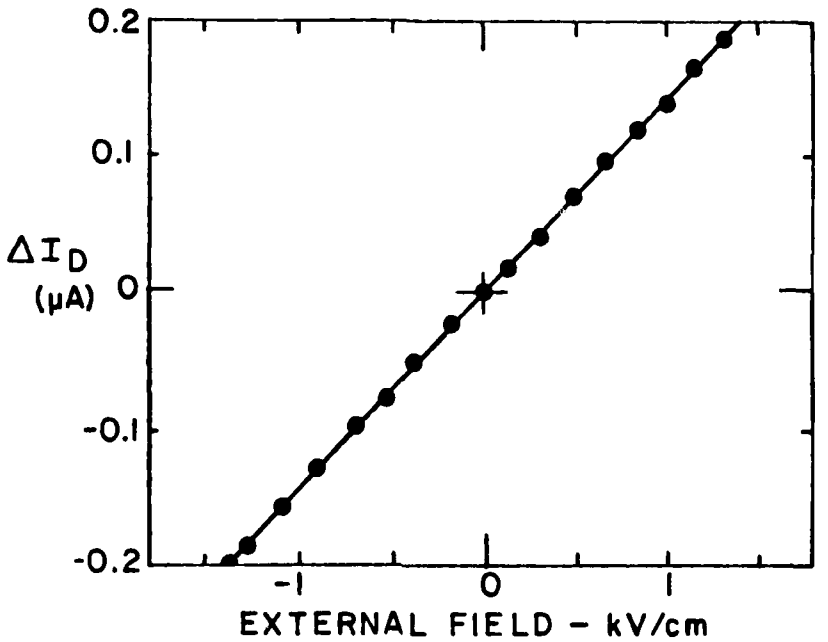


Figure 3.15 Plot of change in FGFET drain current I_D v.s. applied external field E_o.

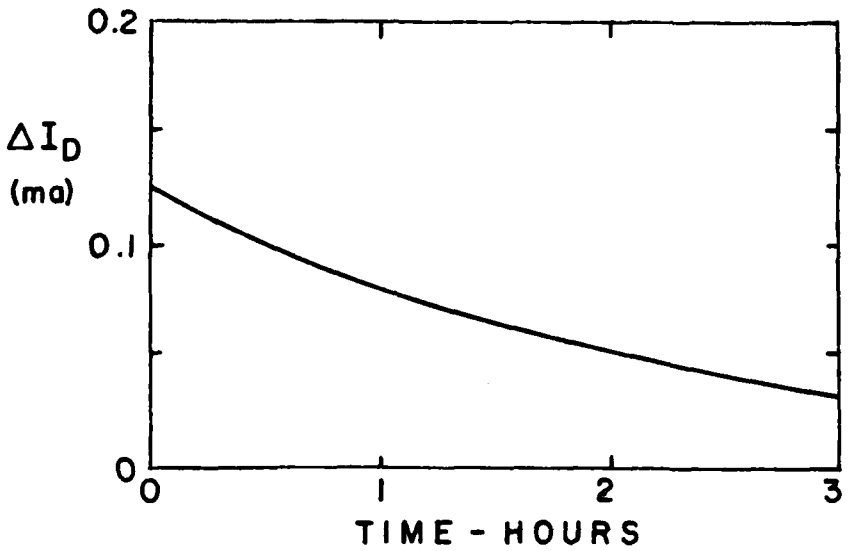


Figure 3.16 Rough plot of FGFET I_D versus time in response to a 10 kV step change in external electric field E_o.

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4. LABORATORY DEVELOPMENT OF THE DGFET

Although the FGFET field sensor offers improved performance over the unmodified MOSFET sensor its RC relaxation time may still be too short for some applications. At the same time, the presence of the floating gate electrode pad, although not connected to an external electrode, does allow the possibility that a damaging ESD puncture of the oxide layer may occur. In an effort to further improve upon the preformance of the FGFET, a device called the Direct Gate Field Effect Transistor, or DGFET, was developed as part of our research effort. The DGFET differs from the FGFET in that the gate electrode pad is completly absent. As shown in Figure 1.3, the external electric field associated with the surface potential to be measured is allowed to land directly on the oxide layer and substrate of the FET structure. Thus the electric field which modulates the channel conduction between drain and source is derived directly from the external field, and need not be induced upon an intervening metalized gate electrode.

4.1 DGFET Fabrication Methods

Because the basic structure of the DGFET device is not available in any commercial MOS part, or as part of any semiconductor device, special fabrication methods were required. Of the several that were attempted, only direct fabrication by a semiconductor manufacturer proved successful.

The first fabrication method attempted involved the physical

scraping away of the aluminized gate electrode on the 2N3797 and the 3N138 transistors. Scraping was performed with the aid of a sharp needle tip mounted on a translation stage micromanipulator beneath both a 40X power binocular microscope and a 100X - 400X power monocular microscope. In all cases the gate electrode was found to be integrally bonded to the oxide layer beneath it, such that "physical scraping", as one might scrape paint from window glass, is not really possible. In addition, the needle tips employed, which were the sharpest available to us, did not have sufficiently small spatial resolution to allow for pinpoint contact with the gate electrode only. Thus, the source and drain electrodes on devices subjected to the scraping procedure were often damaged. In summary, no success was acheived in using the scraping method to remove gate electrodes.

Another unsuccessful fabrication method involved the etching away of the metalized gate electrode by immersing the MOSFET in an appropriate electrolyte solution. The etching scheme utilized in these experiments is depicted in Figure 4.1. The electrode material to be etched is aluminum and the chosen electrolyte NaOH. The biasing voltage V_1 protects from etching any electrodes that are to be left intact and thus must be kept greater than the electrochemical potential between the metal electrode material and the electrolyte solution. The purpose of the voltage V_2 is to enhance the potential between the electolyte and the metalization areas to be etched. Note that if the voltage V_2 is not connected to these areas, they may be protected

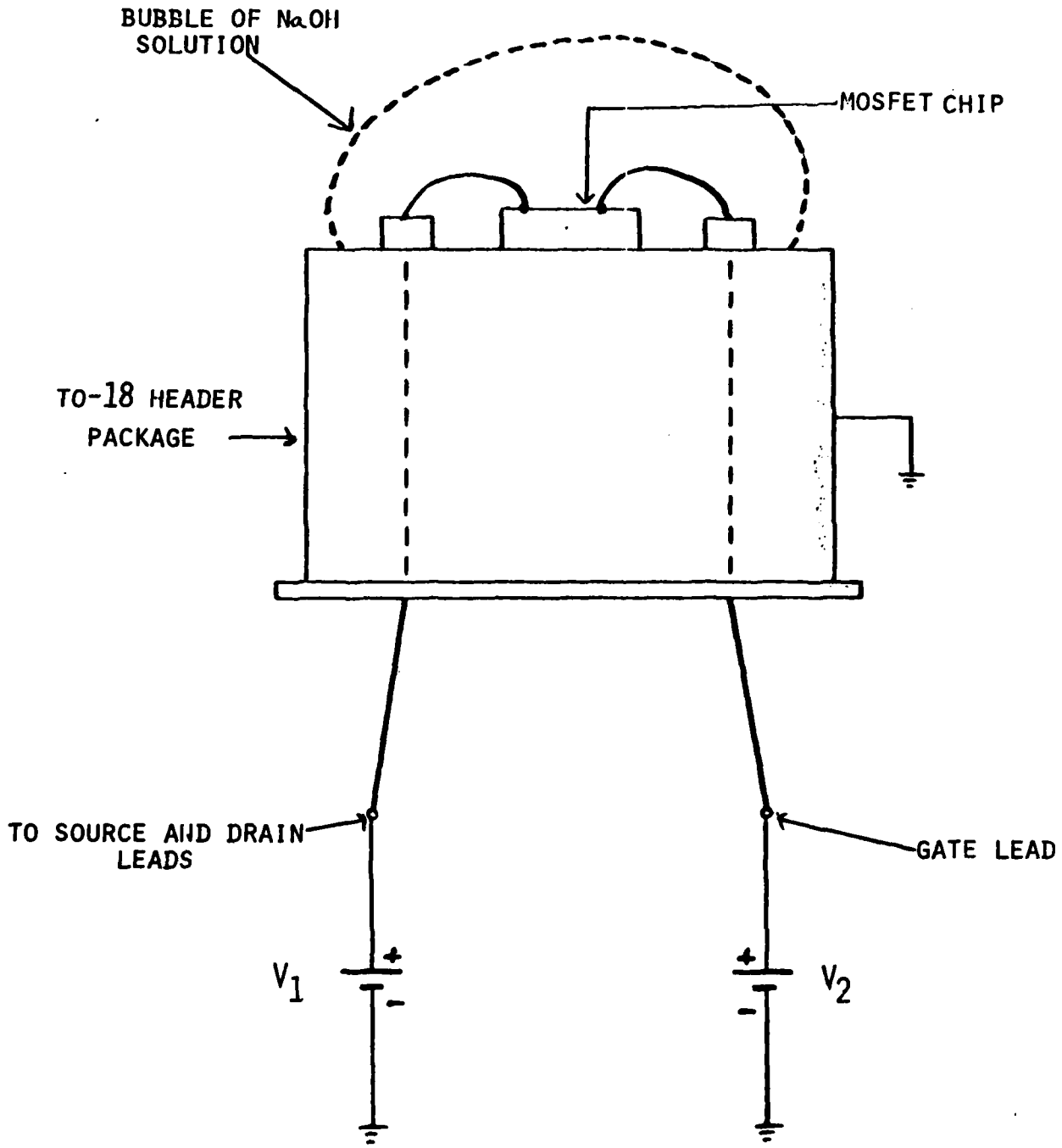


Figure 4.1 Etching scheme used in attempt to create DGFETs from MOSFETS.

from the etching process by V_1, since they are resistively coupled to V_1 through the electrolyte.

Initial success was achieved in attempts to etch away the electrode pads of 2N2222 bipolar transistors (BJT's). These devices were initially employed for testing the etching process because they are much less expensive than MOSFETS. The achieved success in the selective etching of either the base or the emitter contact pads on the BJT can be attributed to the fact that the entire area of each metalized electrode on the BJT is continually kept in electrical contact with its respective bonding wire by the implantation layer lying directly beneath the electrode. Thus continual contact is maintained between the biasing voltage and the electrode material to be etched during the entire etching process.

In contrast, the gate pad of the MOSFET is completely insulated from the substrate of the transistor and the only electrical contact to it is its own through bonding wire. When the etching method is attempted on MOSFETS etching is not observed to occur on the entire gate pad, but only on a small protion of the gate pad leading from the bond wire to the bulk of the pad area. In essence, the gate pad disconnects itself from the bonding wire. The hypothesized reasons for the selective etching of only this narrow neck of the gate electrode pad can be summarized as follows: When the gate electrode is biased by the voltage V_2, the etching begins to occur. The area of highest current density to the gate metalization is the narrow portion just adjacent to the pad area; hence etching at this location

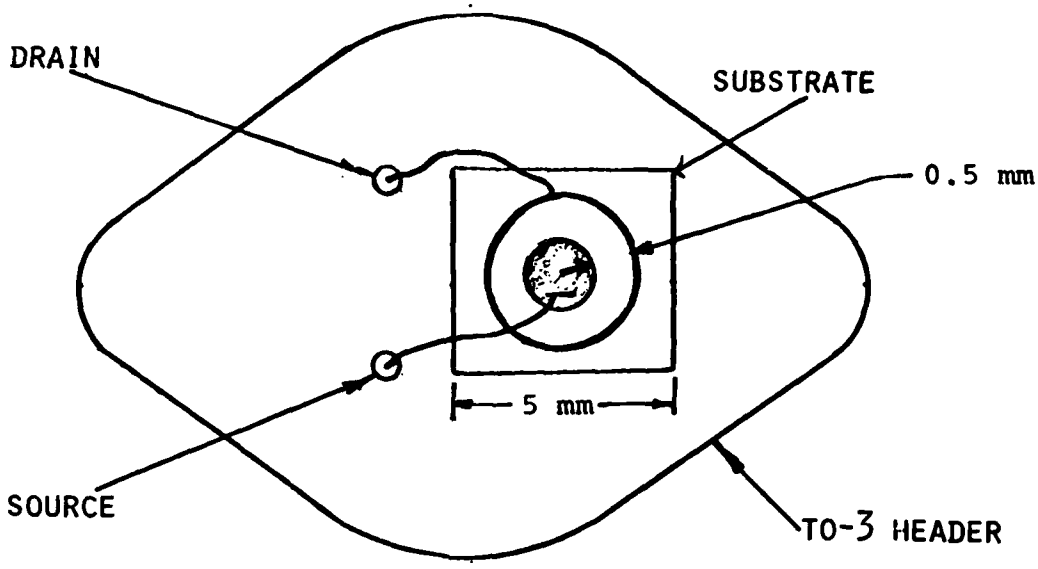
occurs at the fastest rate. Once this area is etched away, the remainder of the contact pad becomes disconnected from the biasing voltage V_2, and etching stops.

In the long run, all efforts to construct DGFETs from MOSFETs failed, and true direct gate DGFET structures had to be obtained from a local manufacturing firm. In our case, Unitrode Corporation in Waltham, Mass. was quite cooperative and fabricated DGFET devices to our specifications. Asketch of the devices fabricated by Unitrode, together with a table of their parameters and specifications, is given in Figure 4.2. Note that the devices supplied by Unitrode are of the depletion mode family, with an oxide layer charge Q_{ss} implanted in the oxide layer.

4.2 Experimental Observations of DGFET I-V Characteristics

When the characteristic curve of the DGFET is displayed on the curve tracer, the peculiar shape associated with the FGFET no longer appears. Rather, as shown in Figure 4.3, the DGFET I-V curve has the form of an unmodified FET operating curve with V_{GS} set to zero. The absence of the self induced gate voltage effect, observed on the FGFET, can be attributed to the lack of the metalized gate electrode on the DGFET, an observation which lends support to the model developed in Section 3 for FGFET behavior.

It should be noted that the general level of operating point drain current, for the DGFET, with no external field applied, is only about 0.5 mA for V_{DS} = 5 volts in contrast to about 5 mA for



DGFET PARAMETERS: (N-CHANNEL)
BORON DOPED 6-9Ω-cm P-TYPE SUBSTRATE
1500 Å OXIDE LAYER
10 MICRON PHOSPHORUS DIFFUSED DRAIN AND SOURCE JUNCTIONS

Figure 4.2 Layout and metalization pattern of DGFET fabricated by Unitrode Corporation.

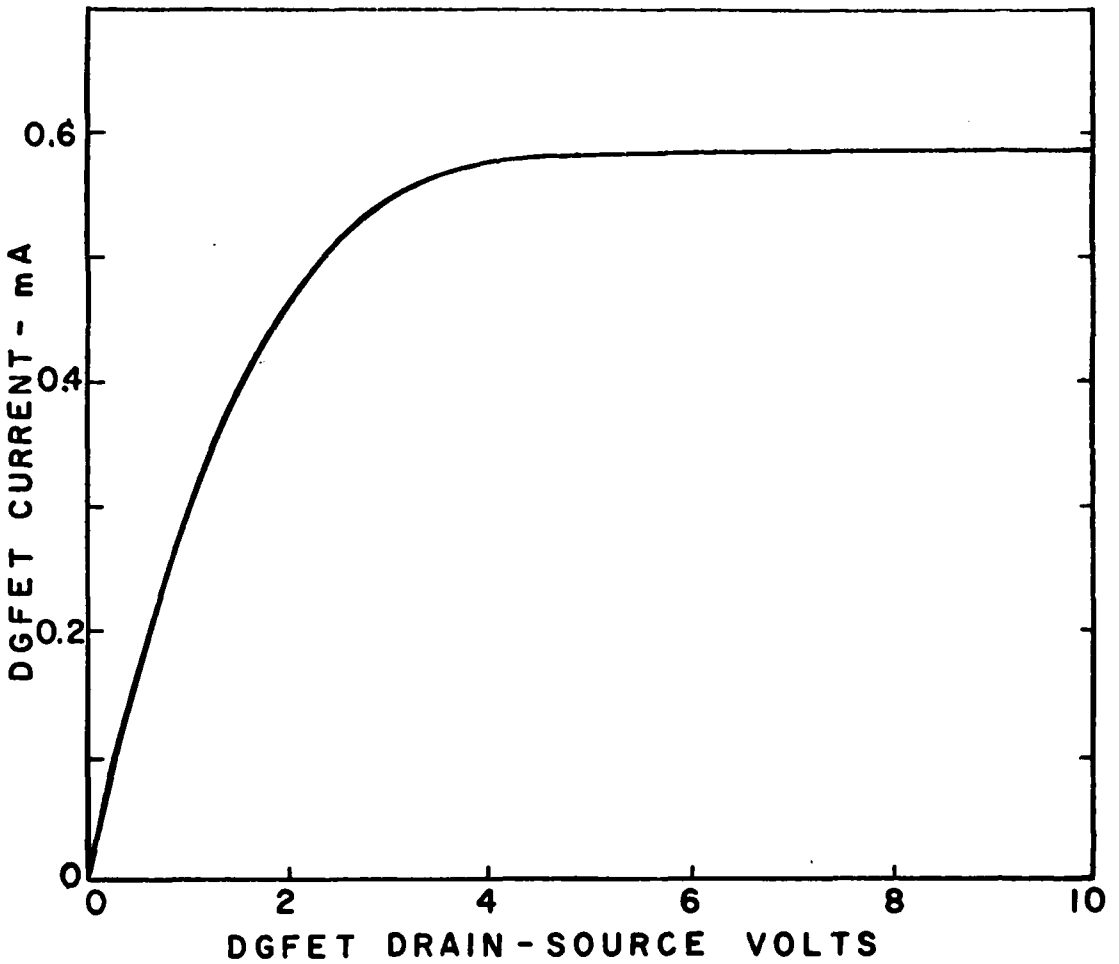


Figure 4.3 DGFET I-V curve as observed on curve tracer.

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the FGFET. The reason for this reduced level of operating point current is assumed to be due to the specific parameters and geometry of these specific DGFET devices. It is presumed that with proper selection of fabrication parameters, larger current levels could be achieved on the DGFET.

4.3 Theoretical Model for the DGFET Device

Because of the absence of the metalized gate electrode, the theoretical model for the DGFET differs slightly from that of the FGFET. The lumped capacitor model discussed in Section 3.3, for example, can no longer be valid. Rather, a distributed capacitance-resistance model must be exclusively employed. Although the specifics of such a model were not examined with the same theoretical detail applied to the FGFET, the qualitative experimental ramifications are evident. First of all, the self induced gate voltage effect observed on the FGFET should be absent. Indeed the shape of DGFET I-V characteristic, shown in Figure 4.3, appears as the curve one would expect from a regular unmodified MOSFET with gate voltage set at zero.

Secondly, the absence of a gate electrode dictates that any charges which flow to the top of the oxide layer, to screen out externally applied electric fields - i.e., charges that participate in the relaxation effect - must flow over the entire surface or bulk of the oxide layer, rather than to the point of closest proximity of a metalized gate electrode. Thus the inherent resistive leakage path in the DGFET should be longer than in the FGFET. Although the capacitance between the surface

of the DGFET oxide layer and the substrate is a distributed function, its integrated contribution will be on the same order as the lumped gate to substrate capacitance of the FGFET. Thus the relaxation time associated with the DGFET is much longer than that of the FGFET. As a result, the ability of the DGFET to maintain a reading from a true applied dc field is greatly enhanced.

4.4 Response of DGFET to Applied Electric Fields

Several DGFET devices were tested using the same electrode configuration of Figure 3.14, that was employed in the FGFET and unmodified MOSFET tests. As can be seen from the graph of Figure 4.4, the sensitivity of the DGFET to the applied field is much less than that of the FGFET, so that more overall amplification must be incorporated into any instrument utilizing the DGFET sensor, if fields of similar magnitude are to be monitored. The plot Figure 4.5 shows the response of the DGFET current to an electric field switched on at t=0. The relaxation effect is evident, but in this case the time constant is on the order of fourteen hours, in contrast to about three hours for the FGFET device.

One disadvantage of the DGFET is that it is sensitive to external sources of light. This behavior is not surprising, given that the substrate area is not shielded by an opaque gate electrode. it is hence left vulberable to the photon generation of excess carriers in the channel region between drain and source. In practice, the random signals generated by ordinary room light are seen to be equivalent to surface potentials on the order of several kilowatts.

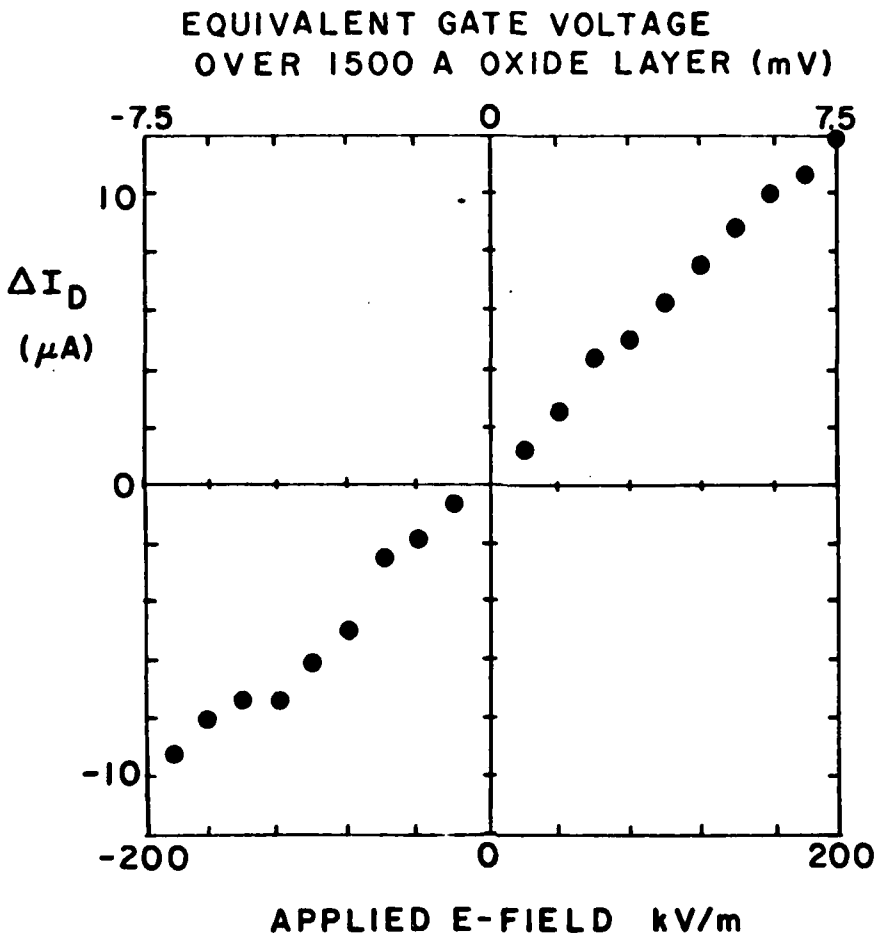

Figure 4.4 Plot of Change in DGFET drain current I_D vs. applied external field E_y. Upper scale shows equivalent "gate" voltage that would have to be applied to a regular MOSFET to achieve same oxide layer field.

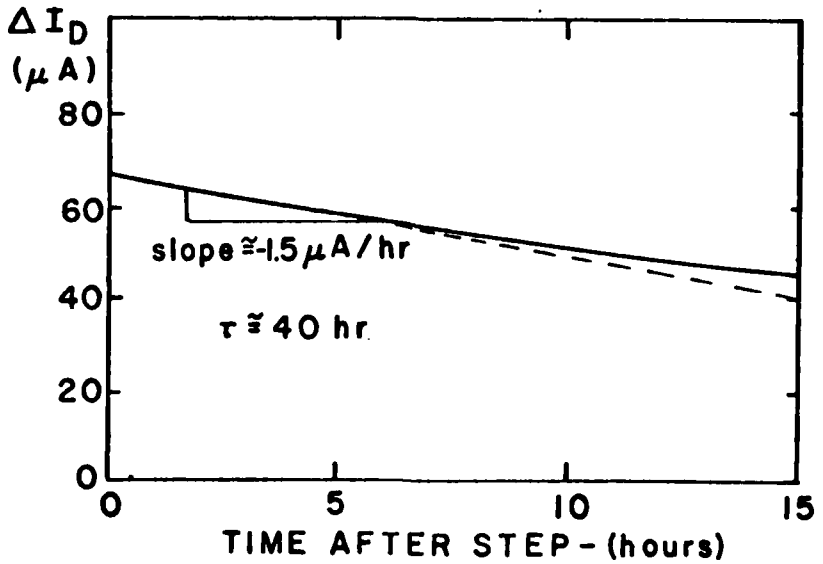

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Figure 4.5 Rough plot of change in DGFET current versus time, in response to a step change in electric field.

5. STABILIZATION OF SENSOR OPERATING POINT

One problem that was encountered in the early stages of FGFET and DGFET development concerned the drift of the device operating point with changes in ambient temperature. An example of the problem is shown in Figure 5.1, which shows plots of the operating point of one FGFET device versus time, with no external field applied, and with the device sitting on the lab bench. The output is seen to drift more or less in concert with changes in temperature. Such behavior is not surprising, given the generally known sensitivity of semiconductor parameters to temperature, and the low signal levels that are of interest. Two approaches were taken in an effort to control the problem of temperature sensitivity.

5.1 Selection of Matched Pair Devices

One approach to the temperature problem involves the use of a reference device, not exposed to the field, but kept at same ambient temperature as the actual sensor. If both devices are matched for temperature coefficient, then temperature dependence should be a common mode signal that is cancelled out. The difference in operating point between devices can then be interpreted as an output signal proportional to the external field.

A batch of about one hundred 2N3797 transistors were thus carefully measured for operating point characteristics and temperature coefficient, and grouped into pairs of closely

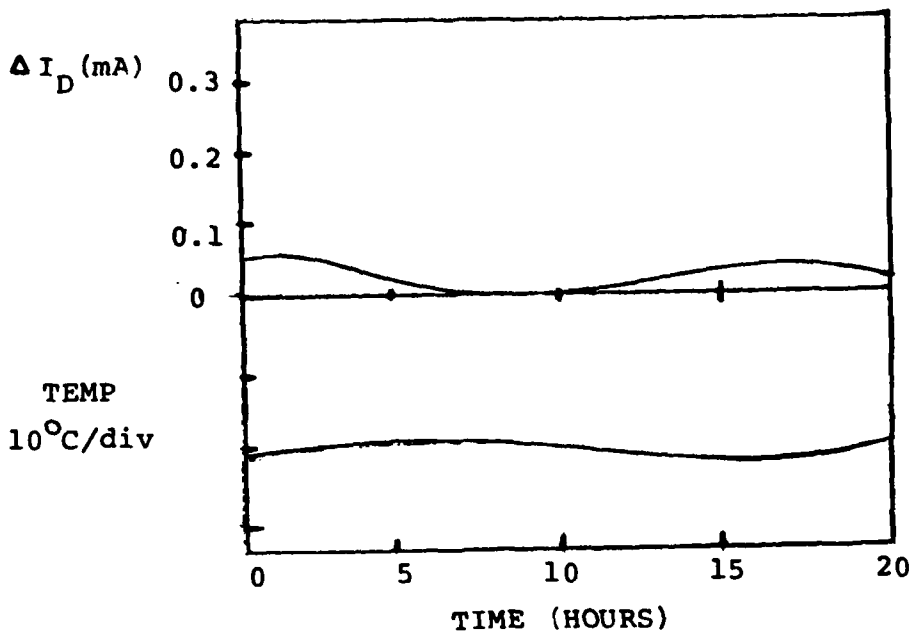

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Figure 5.1 PGFET operating point versus time with no external field applied. Absence of stability is evident.

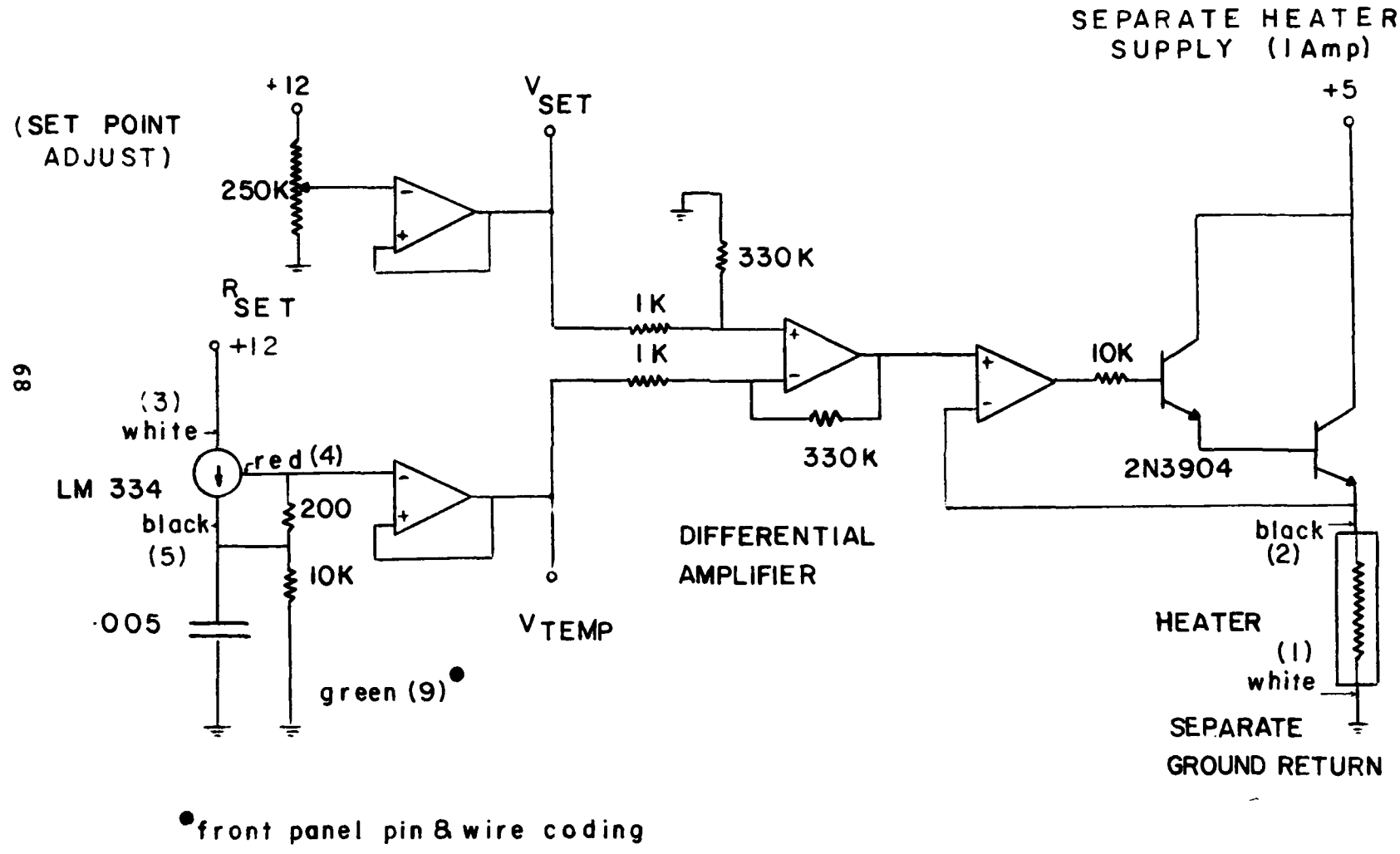
matched devices. As discussed in Quarterly Reports #2 and #3, utilization of such "matched" reference devices did improve overall instrument insensitivity to temperature by about a factor of four, but device matching, whcih was not perfect, was insufficient to allow for complete cancelling of all temperature effects.

Better matching might be possible with "die matched" pairs of devices - i.e. matched transistors taken from adjacent dies on the same silicon wafer. All attempts to procure such devices were unsuccessful. We could not, with the time frame of the research project, find any source of truly die matched parts.

5.2 Active Temperature Control Scheme

As a next step in device stabilization, a system was devised to keep both the sensor and reference at the same approximately constant temperature, set several degrees above ambient room temperature. A circuit schematic of the system developed is shown in Figure 5.2. (The details of transistor mounting on the thermal control block will be covered in Section 6.) The system is capable of holding the transistor case temperature to within $\pm$ ^{o}C of the equivalent set point temperature. Utilization of this thermal control system was successful in reducing the temperature problem significantly, as is evident in the plot of Figure 5.3, which shows the output of a FGFET versus time, with the thermal controller at work (no external field applied).

An LM334 integrated constant current source was chosen as the thermal sensor. The voltage appearing across the biased network of this device varies linearly with the temperature, with



●front panel pin & wire coding

Figure 5.2 Thermal control system.

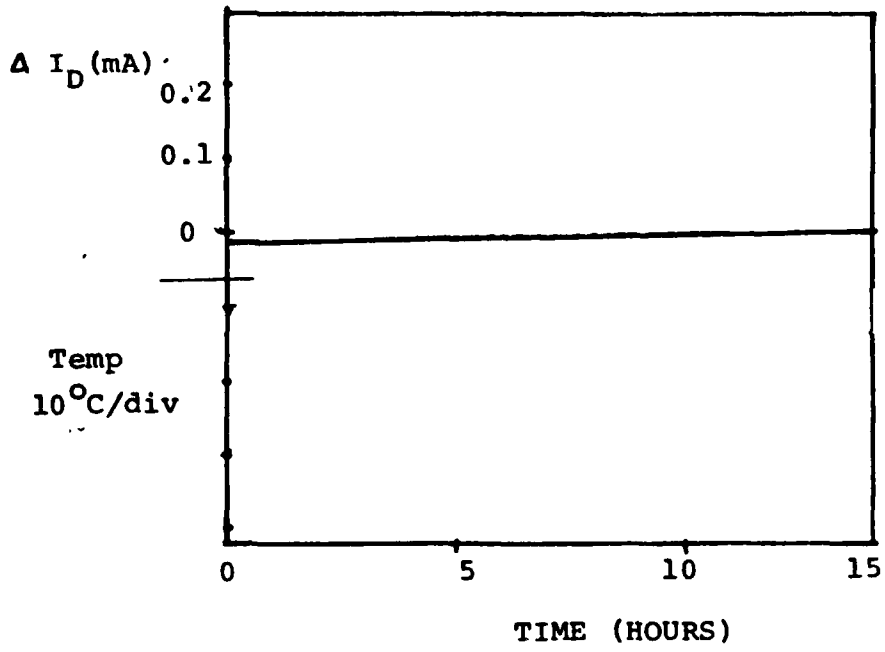


Figure 5.3 Plot of FGFET operating point versus time with thermal controller at work.

a slope of about 0.08°C/mV, and an output at room temperature of about 3.35 volts. In operation, the set point of the thermal controller, determined by the potentiometer R_{SET}, is set to several tenths of a volt above the room temperature output voltage of the thermal sensor. The op-amp feedback loop applies power to the heater until the temperature of the thermal block equals the set point temperature. In practice, the temperature of the thermal block is seen rest a few degrees below the set point temperature, probably because of convective and conductive heat losses to the ambient environment. (When the sensor is mounted in a vacuum, the lag between thermal block and set point temperatures is smaller than that experienced in air, because the convective losses are absent).

5.3 Long Term Drift Correction

Although temperature sensitivity is definitely a source of operating point drift in both the FGFET and DGFET devices, several other drift mechanisms seem to be at work also. Although these mechanisms are not clearly understood at this point in time, they may involve such phenomena as surface ion migration within the oxide layer or changes in the oxide layer surface resistivity, which couples the gate electrode to the drain and source leads. Either of these phenomena would change the equilibrium level of gate voltage resulting when a drain to source voltage is applied.

In any case, the drift associated with these "unknown" sources of operating point changes is observed to occur over time

scales comparable to, or greater than, the intrinsic RC relaxation time constant discussed in Section 3.

One approach contemplated for compensating for these extraneous sources of drift in a working surface potential instrument involves the use of an active filter network, which would separate out the extremely low frequency (10^{-5} Hz) drift components,from the relatively higher frequency (10^{-3} Hz) signal components. A block diagram of the system envisioned is shown in Figure 5.4. Implementation of this scheme was attempted as part of Ed Walsh's Master's Thesis (Appendix D). Although some preliminary success was achieved, no conclusive results have been obtained to date. Nevertheless, the scheme may be worthy of future investigations as a method for improving upon field measuring schemes utilizing the FGFET and DGFET.

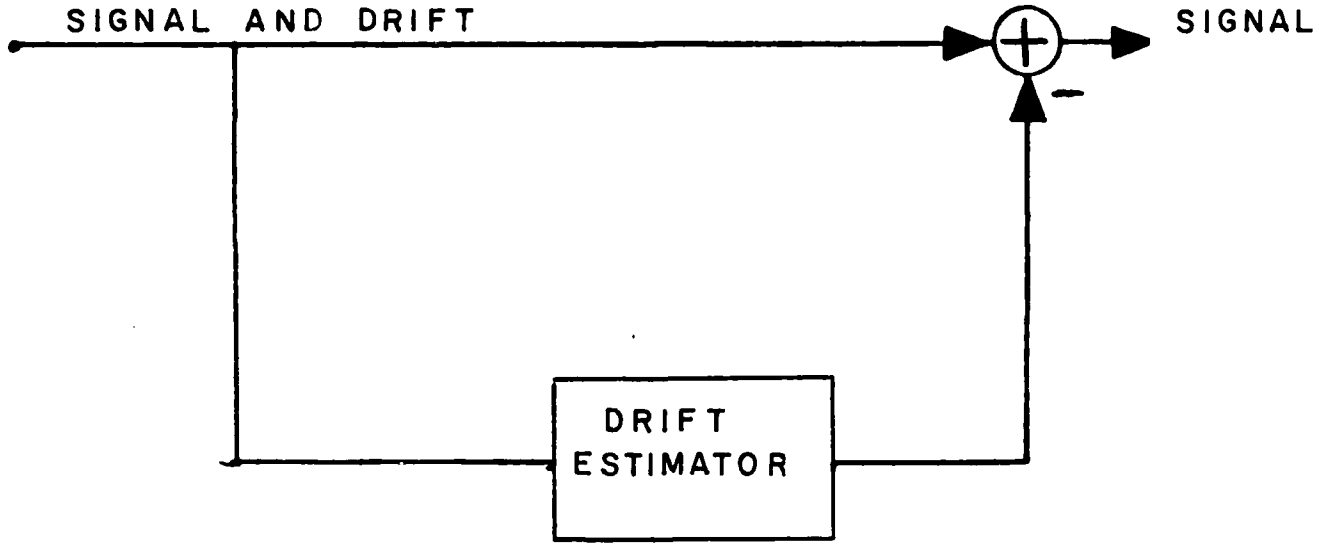


Figure 5.4 Block diagram of long term drift compensation scheme.

6. DEVELOPMENT OF ACTUAL TEST INSTRUMENT

6.1 Probe Head Designs

As of the writing of this report, two working probe heads, one each incorporating the FGFET and DGFET sensors described in the previous sections, have been delivered to AFGL. The criteria to be met in the final design of the probe head included the utilization of an overall electrode configuration that would minimize the chances of arcing from surfaces of high potential or static charge, as well as the use of well shielded sensor and reference transistors. In addition, the thermal controller described in Section 5 was incorporated directly within the probe head to aid in the maintaining of device operating point stability. After several designs on paper, the geometrical configuration shown in Figure 6.1 was chosen to maximize proper field grading at the edges of the probe head. The radius of curvature of the torus was selected to match a probe-to-surface gap of approximately 5-10 cm.

Figures 6.2 and 6.3 show the sensor mounting details in the FGFET and DGFET probes respectively. In each case, the sensing transistor sits beneath in a 1" aperture in the center of the probe face, atop the thermal controlled block, which is made from a machined TO-5 transistor package. The copper mounting slab inside this particular transistor package provides an excellent thermal mass for the operation of the thermal control system.

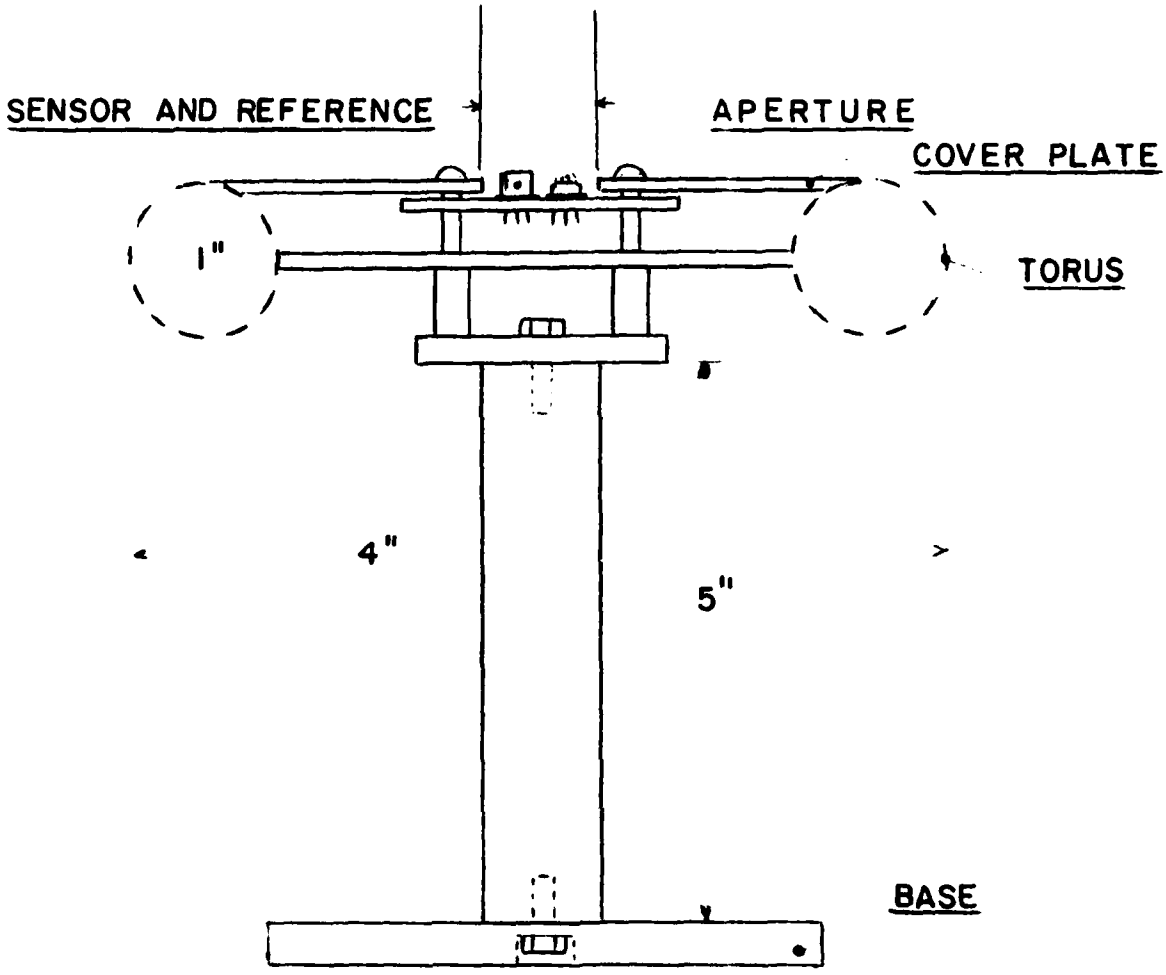


Figure 6.1 Geometrical design of surface potential probe head.

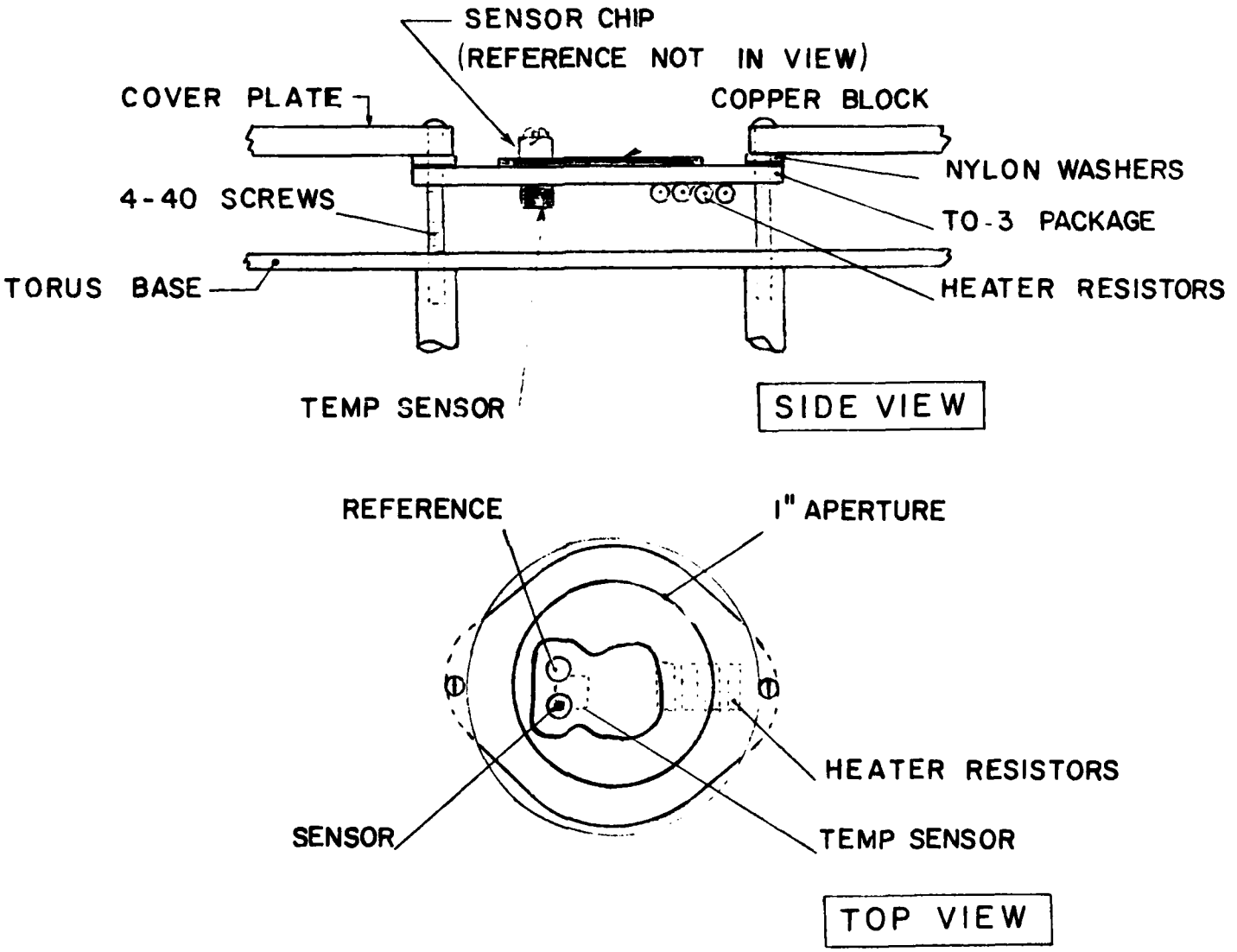
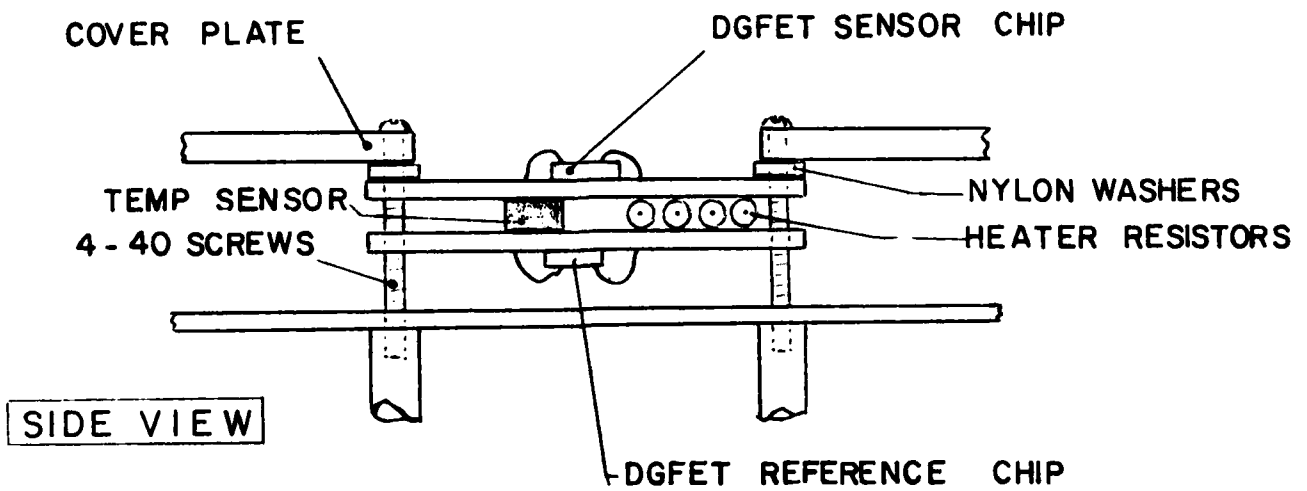


Figure 6.2 Mounting details in FGFET probe.



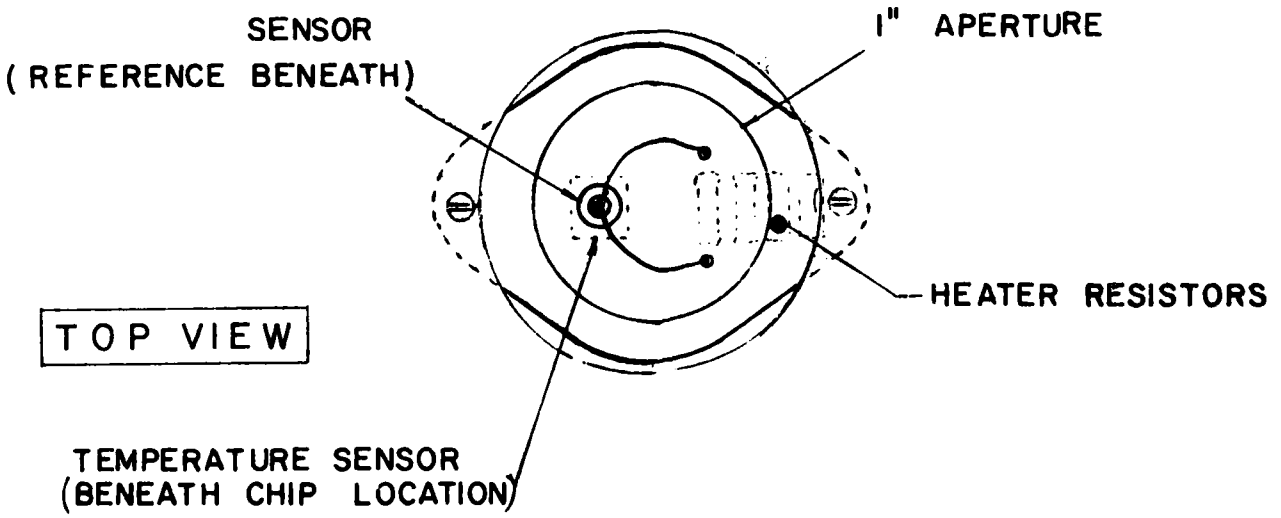


Figure 6.3 Mounting details in DGFET probe.

Although the thermal control block is electrically connected to the probe shell, it is thermally isolated from it, so as to minimize conductive heat loss to the probe body. This thermal isolation, together with the necessary electrical contact between the block and the probe body, is implemented by the insertion of nylon washers between the thermal control block and the inner edge of the probe head. Since the screws are metal screws, electrical connection is maintained, but the the thermal conduction path is minimized. The details of this mechanical mounting scheme can be seen in Figures 6.2 and 6.3.

In the case of the FGFET probe, the reference transistor is mounted next to the sensor transistor. Its transistor case cover is left intact, however, so that the electric field to which the probe head is exposed can not land on the reference transistor chip. Thus only the sensor chip "sees" the electric field, while both sensor and reference are kept at the same approximate temperature by the thermal control block. In the case of the DGFET probe head, the reference transistor is mounted directly beneath the sensor transistor, but pointing in the opposite direction, so that it too is not exposed to the external field landing on the sensor transistor.

Initially, it was thought that the preamp circuitry interfacing the sensors to the synchronous detector (see Section 6.2) could be mounted inside the probe head. However, this circuitry proved to be too complex to allow such mounting, given the electronic fabrication capabilities of our laboratory, and the limited space within the probe head. In the future, such mounting might be possible, and even advisable, if flat pack

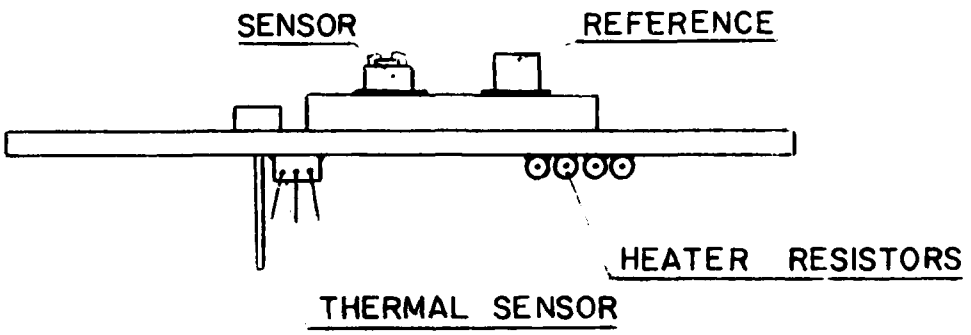


Figure 6.4 Location of various components of the thermal control system. as mounted on the underside of the thermal control block. FGFET probe is shown; DGFET is similar.

operational amplifier packages are used. In our case, however, it proved adequate to simply connect the various sensor and reference leads remotely to the interface board within the synchronous detector via coaxial cables. Note that although the sensor source leads are kept at quasi-ground potential by the input circuitry at the interface board of the synchronous detector, they do carry signal currents. Hence the shield wires leading from each source connection at the probe head must be kept insulated from ground.

The location of the temperature sensor mounted on the underside of the temperature control block in each probe head can be seen examining the details in Figure 6.4. The wires connecting the LM334 temperature sensor and the heater resistors, to the rest of the temperature control circuitry located inside the synchronous detector chasis, extended out the bottom of the toroidal electrode. All thermally related components, including the LM334 temperature sensor and the heater resistors, are attached to the thermally controlled block using cyanoacrylate adhesive. After a suitable bake out period under which can be initiated by energizing the heater the adhesive exhibits minimal outgasing under vacuum conditions.

In operation of the surface potential monitoring system, it is intended that the probe head be mounted such that its face is situated about 5 cm from the surface under test. The method of mounting is not critical so long as all mounting hardware is kept away from the proximity of the sensor aperture. Calibration of the probe head is performed with the

assumption that the field extending between the probe head and the surface under test is undistorted by extraneous metallic materials.

6.2 **Interfacing with Synchronous Detector**

From the outset of the project, the use of a synchronous detection system was intended as a means for extracting extremely low level readings from the sensor signals. An additional advantage of synchronous detection, which became apparent, however, was the possibility of using low level ac excitation for the sensor and reference, which helped control the thermal stability problem by minimizing the direct electrical power input to the transistors, and eliminated the need to energize the devices with a dc drain-source voltage.

The theory of synchronous detection is discussed in Appendix B, while the specific operating and design principles of the synchronous detector supplied to AFGL are given in Appendix C. Hence, only the basic concepts of synchronous detector interfacing will be discussed in this section. The synchronous detector generates a synchronizing signal which must coordinate the energization of the drain-source voltage the sensor and reference. The interface circuit which accomplishes this task, and monitors the resulting drain current to both the sensor and reference, is shown in Figure 6.5. A set of ten binary DIP switches digitally selects the peak excitation voltage to be applied to both sensor and reference. This digitally selected voltage is then fed to a digital to analog converter (D/A), which

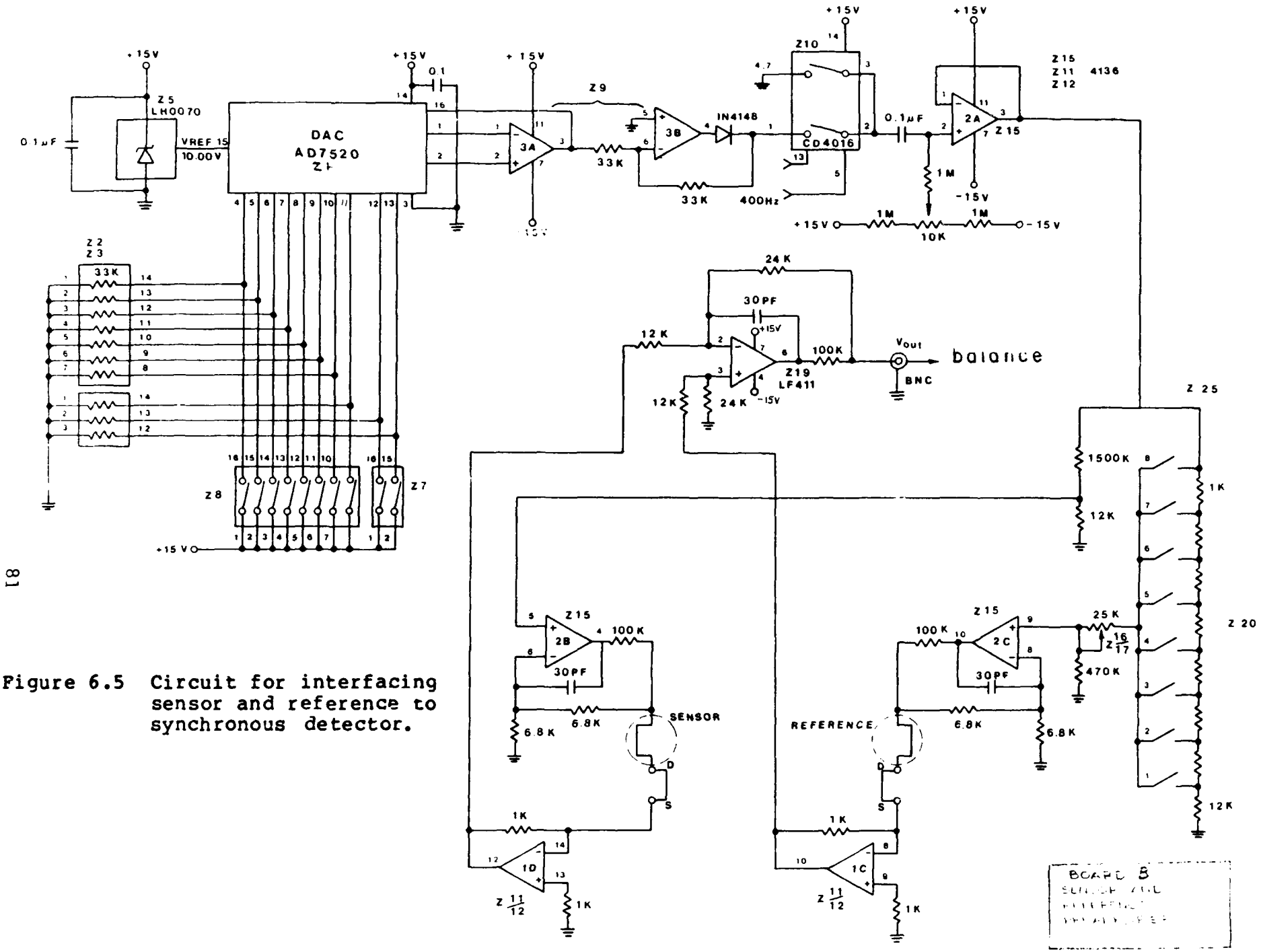


Figure 6.5 Circuit for interfacing sensor and reference to synchronous detector.

converts the digitally coded switch settings to an analog voltage between zero and ten volts. Because ten bit conversion is used, analog voltages as low as ten mV can be obtained. This voltage is next fed to a choppping stage, which converts it into a symmetrical ac voltage with the same peak to peak value as the dc voltage. The chopping frequency and phase are determined by reference signals derived from the synchronous detector, as discussed in Appendix C. In our case the chopping is 400 Hz.

As discussed in section 3.3, a dc bias voltage applied initially to the FGFET sensor will initiate an exponential transient as the dc component of induced gate voltage, resulting from the applied drain-source voltage, begins to relax from its capacitively determined to its resistively determined value. It is critical, therefore, that the dc component applied to the FGFET sensor be minimized. Thus after the chopping operation, the excitation signal is fed through an offset stage, which cancels any dc component added to the signal by the operational amplifiers. This signal is then fed to a balancing stage, which compensates for any mismatch that exists between the sensor and reference devices. Coarse matching is accomplished by a precision resistor network, accessed by a set of binary dip switches, as shown in Figure 6.6. A potentiometer, or variable resistor, was not used for this purpose because of the need for extreme stability of the coarse setting. The fine adjustment, on the other hand, is accomplished with the use of a ten turn pot located on the front panel of the synchronous detector (labled "ZERO"). The value of the resistors in the precision network are chosen so that successive switches yield a jump in range

approximately equal to that of the entire range of the fine adjustment potentiometer. Finally, this excitation signal is fed, via buffering op-amps, to both the sensor and reference respectively. The currents flowing to the sensor and reference, as a result of these excitations, are monitored by current sensing op-amps, whose signals are fed to a differential amplifier, which rejects the common mode between them. The difference signal, which thus consists of a chopped wave form synchronized to the frequency of the synchronous detector, and of amplitude proportional to the external field, is sent to the range amplifier stage of the synchronous detector.

During the calibration phase of both the FGFET and DGFET probe heads, various combinations of device excitation level and synchronous detector gain were tried. Optimization was accomplished by a trial and error method. The results of these tests are summarized in Table 6.1, which lists the various synchronous detector settings that yield good results when the probes are used to measure electrostatic fields. Also included in the table are the minimum sensitivity and the maximum sensitivity achievable with each type of sensor head. The minimum sensitivity is equal to the surface potential represented by one count on the digital output meter of the synchronous detector. In practice, sporadic noise jumps equal to one or two times this minimum value may be observed. Note that in both cases, the minimum sensitivity value is well below the 200 Volt minimum specified in the original project proposal.

The high end of the potential measuring scale is in reality

limited by the probe-to-surface spacing, and not by the probe head or synchronous detector. With the specified spacing of 5cm potentials up to the 20 kV range can be monitored by simply reducing the gain setting of the synchronous detector. Higher potentials could actually be measured by the detector, but arcing to the probe head would be likely to occur. Increasing the distance between the probe head and the surface should make possible the measuring of higher potentials. However, recalibration of the field measuring system would be required at larger gap settings, because calibration was performed at the specified five centimeter gap setting.

Table 6.2 lists the various size and power specifications of the detector system, while Table 6.3 compares the power requirements of this system to other commercial vibrating reed type surface potential monitor instruments.

Table 6.1 - Optimum Settings of Synchronous Detector

	FGFET Probe	DGFET Probe
Gain	#3 (x50)	#4 (x100)
Excitation	Switch 8	Switches 6 & 8
Balance	Switch 6	Switch 6
Integrator Capacitor	A (1μF)	A (1μF)

Table 6.2 - Specifications of Surface Potential MOnitor System

	Probe Head	Synchronous Detector
Size:	4" (8.2 cm) diameter 6" (15.2 cm) tall	19" x 5.5" x 12" (48 cm x 14 cm x 30 cm)
Weight:	approximate 0.5 lbs (.23 kg)	approximately 4 lbs (1.8 kg)
Power Consumption:	Sensor and Reference about 10 mW max Heater approx. 3-4 W maximum	Analog Section : 1.3 W Digital Section : 1.7 W Total (Excl.htr.): 3.0 W
Power Requirements:	Obtained from Synchronous Detector	120 Vac - 60 Hz
Output Range @ 5 cm Probe to Surface Distance:	0-20 kV	
Resolution:	200 - 500 V	

Table 6.3 Comparison of Power Requirements for AFGL Surface Potential Probe System with Commercial Vibrating Reed Types

AFGL probe w/o heater	3 Watts
AFGL probe with heater	~6-7 Watts
MONROE Model 244 0-3kV system	15 Watts
TREK 340 HV 0-20 kV system	40 Watts
TREK 320 B 0-200 V system	10 Watts

7. TESTS IN AFGL VACUUM CHAMBER

Although most of the tests reported here were performed in the laboratory at Boston University, final calibration and testing was performed in the vacuum chamber at AFGL. These tests can be considered the bench mark tests for device performance, with all elements of the monitoring system optimized to eliminate or minimize all sources of noise and drift. The difficulties associated with temperature stability, operating point drift, detection methods, and mechanical construction were addressed and rectified as much as possible before the AFGL tests.

The optimized FGFET and DGFET probes performed better in the tests at AFGL than originally expected, given the lack of optimism surrounding the development of the sensors. Although the field monitoring system incorporating the FGFET and DGFET sensors is far from optimal, and certainly not ready for actual space flight, the tests at AFGL were encouraging. Many of the problems associated with the sensors in air seemed to disappear when the probes were placed in vacuum. Although it may be unscientific to say the sensors "like to be in vacuum", this statement is nevertheless true. One possible explanation for the improved performance of the sensors may actually lie in the improved performance of the temperature control system. In the absence of thermal convection as a heat loss mechanism for the sensors, small shifts in temperature, which would cause fluctuations in the device operating points, would be absent.

Such "quieting down" behavior of the sensors was actually observed as the vacuum chamber was pumped down from atmosphere.

Several other theories for improved device preformance in vacuum have also been forwarded, but evidence exists at the present time to either prove or disprove them. Hence, in the remainder of this section, the tests at AFGL will simply be described and evaluated.

7.1 **Calibration Curves**

Final calibration of the probe heads was performed in the vacuum chamber at AFGL. With the probe head situated at 5 cm beneath the energized plate, the output values of the synchronous detector were recorded. Note that the length and width of the energized plate were chosen to be of sufficient dimensions to minimize edge effects between the plate and the probe head. Thus the calibration will be most meaningful in the future when the probe head is used to measure the potential on relatively large surfaces. Calibration of the probe head for use in monitoring smaller surfaces of arbitrary shape is possible if a high voltage electrode of appropriate shape is used.

The calibration curves recorded in the AFGL vacuum chamber are shown in Figs. 7.1 and 7.2.

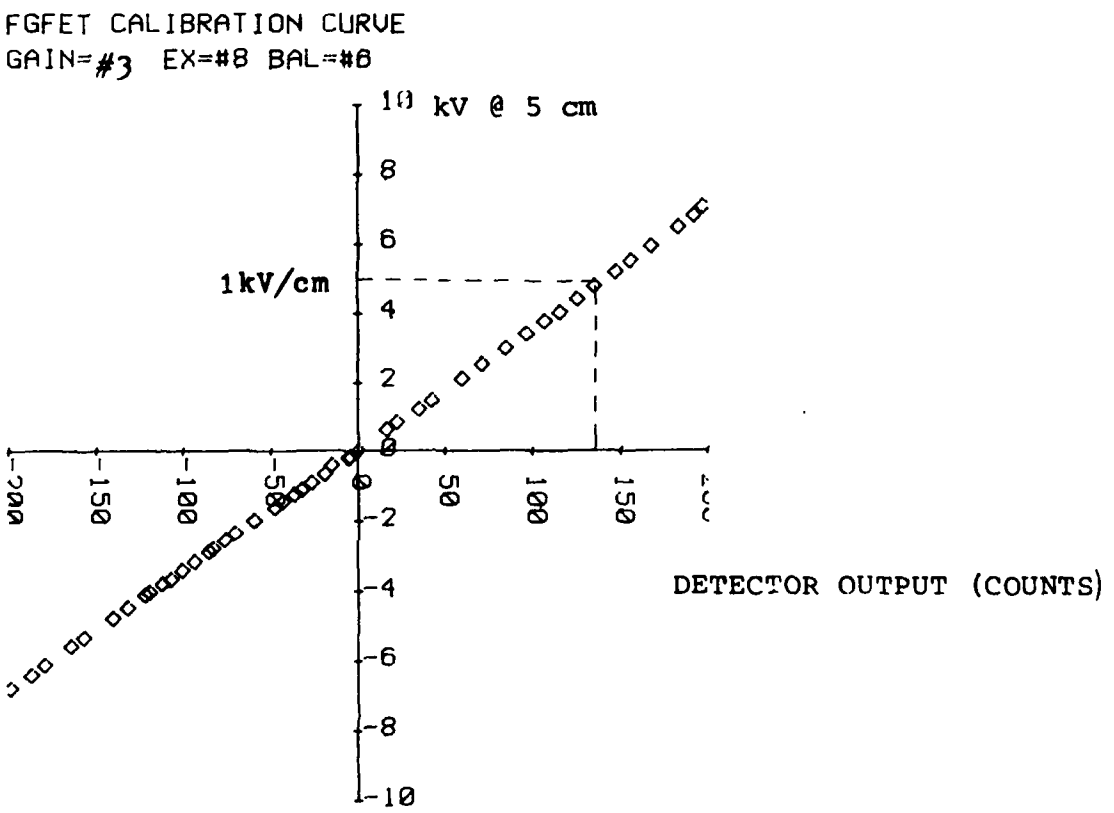


Figure 7.1 FGFET Probe calibration curve @ 5 cm

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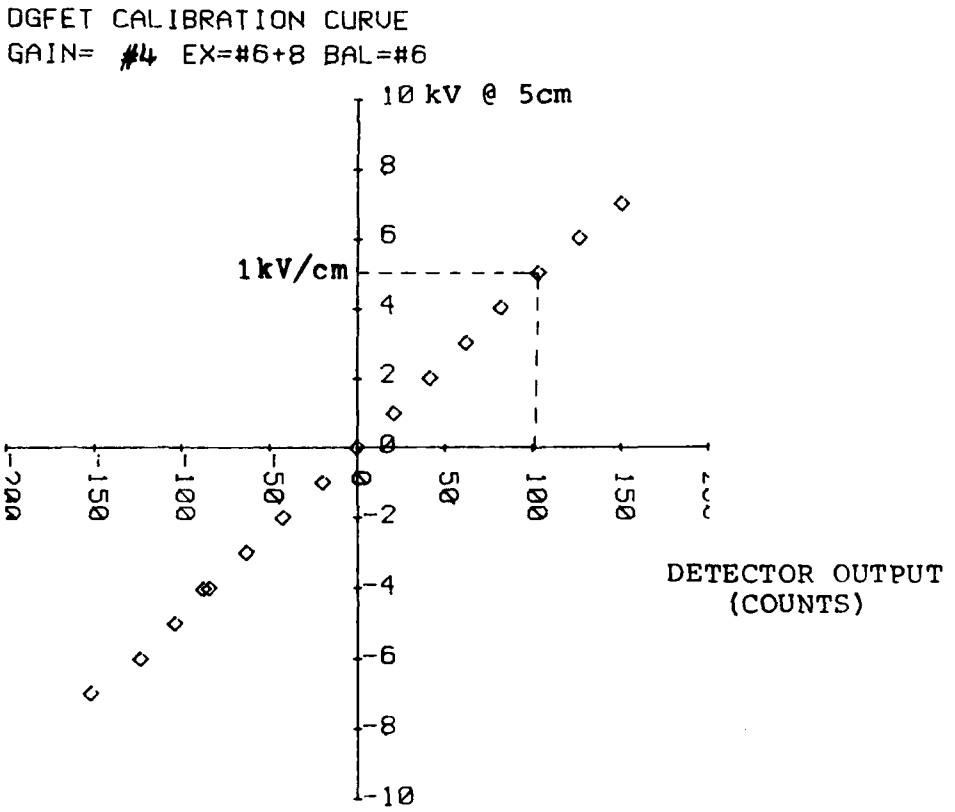

Figure 7.2 DGFET probe calibration curve @ 5 cm

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7.2 **Step Field Energization Tests**

As a method of measuring the relaxation time associated with each sensor type in a vacuum environment, a field step energization test was performed on each. In these tests, the probe head was situated in the vacuum chamber, with the thermal controller turned on, and allowed to come to thermal equilibrium over a period of approximately one half hour. Next, a high voltage potential of 5 kV was quickly applied to an electrode plate situated 5 cm above the probe head, so that a "step" of electric field was applied to the probe. With the output of the synchronous detector monitored by a chart recorder, the field was left energized for a long period of time, usually overnight, so that the decay in the sensor reading could be observed. A plot of such a field energization test for the FGFET is shown in Figure 7.3 and a similar plot for the DGFET test is shown in Figure 7.4. Extrapolations of these tests show the relaxation time constants associated with each sensor to be about five hours for the FGFET and over one hundred hours for the DGFET. Note that these time constants are longer than those experienced with the devices in air a not surprising result, given that much of the surface leakage paths affecting the relaxation time are attributable to moisture collected or absorbed on the oxide layer surface. This surface moisture is quickly evaporated when the devices are situated in a vacuum environment.

7.3 Long Term Stability Tests

As discussed in previous sections, several factors seem to upset the long term stability of the FGFET and DGFET operating points. In an attempt to categorize long term instabilities, a set of tests were run in which the probe head, with thermal controller at work, was exposed to no electric field, and monitored over a period of many hours (typically overnight). The results of such a test for each type of sensor are shown in Figure 7.5 and 7.6. Note that in contrast to previous tests performed in air, the drift experienced over a long period of time in the vacuum chamber represents an equivilent surface potential of only about 500 volts. Any drift representing equivalent potentials larger than this value occur over periods of time that are longer than the hour or so monitoring times of interest.

One possible explanation for the reduced sensor stability in air may be the presence of air ions which land on the sensor surface, and thus cause extraneous output voltages to appear. Another explanation for reduced stability in air may be that exposure to air causes long term changes in resistive coupling which couples the gate to source and drain leads, leading to an apparent drift in the output of the synchronous detector.

7.4 Result of Accidental Vacuum Arc

During the course of the experiments in the vacuum chamber, two accidental vacuum arcs were experienced. Although this topic

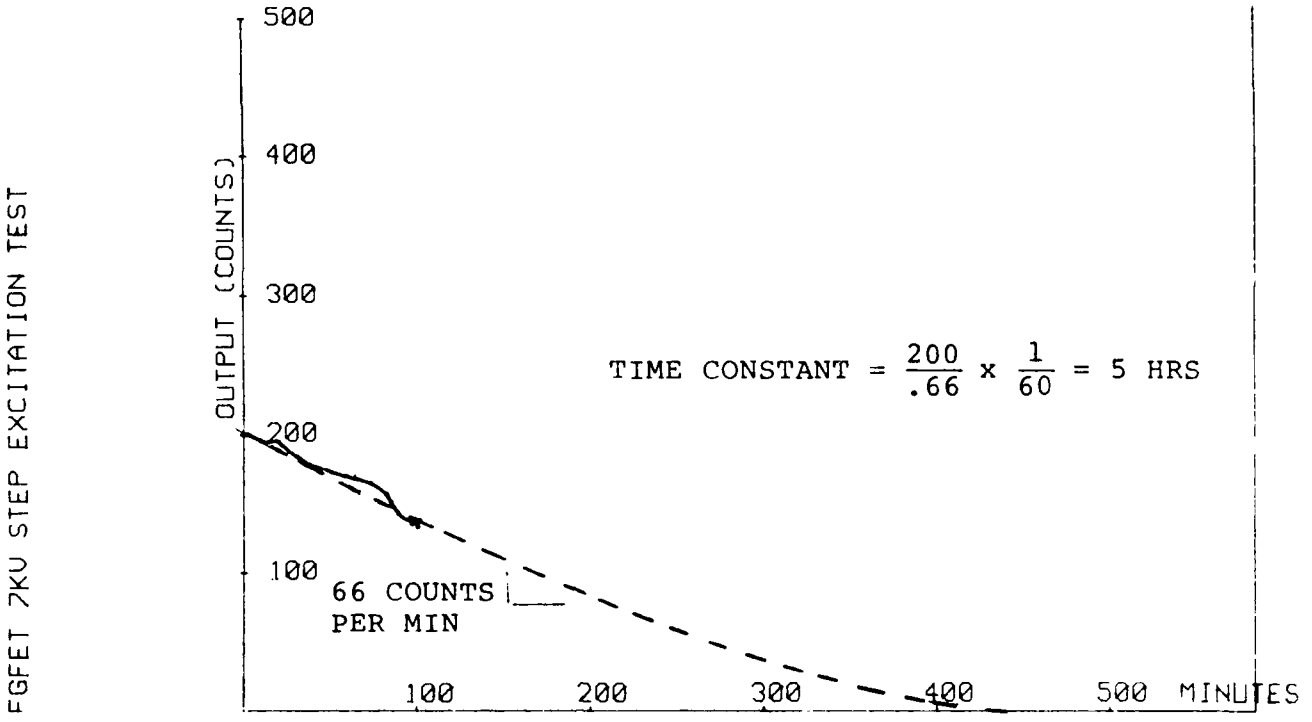

Figure 7.3 Step field energization test on FGFET probe 7 kV step.

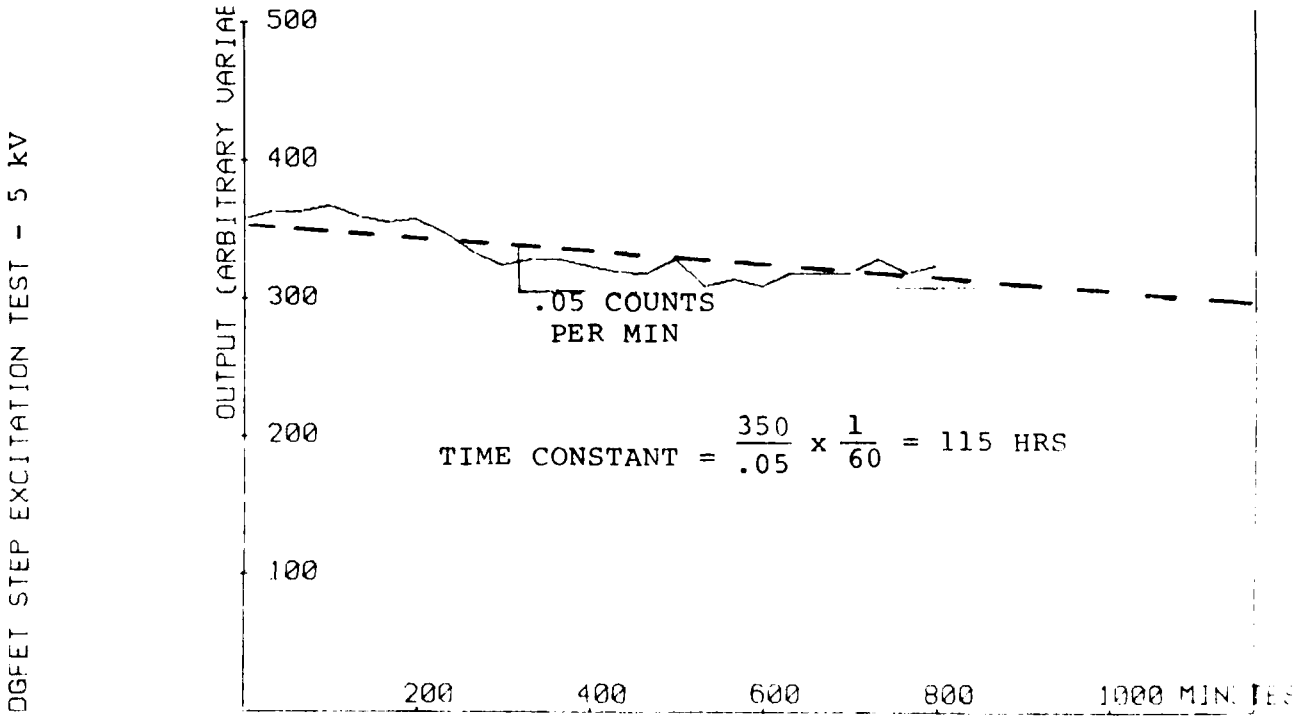

Figure 7.4 Step field energization test on DGFET probe. 5 kV step.

AD-A140 024 A PROBE FOR MEASURING SPACECRAFT SURFACE POTENTIALS USING A DIRECT-GATE F..(U) BOSTON UNIV MA M N HORENSTEIN ET AL. 30 SEP 83 AFGL-TR-83-0255 2/3

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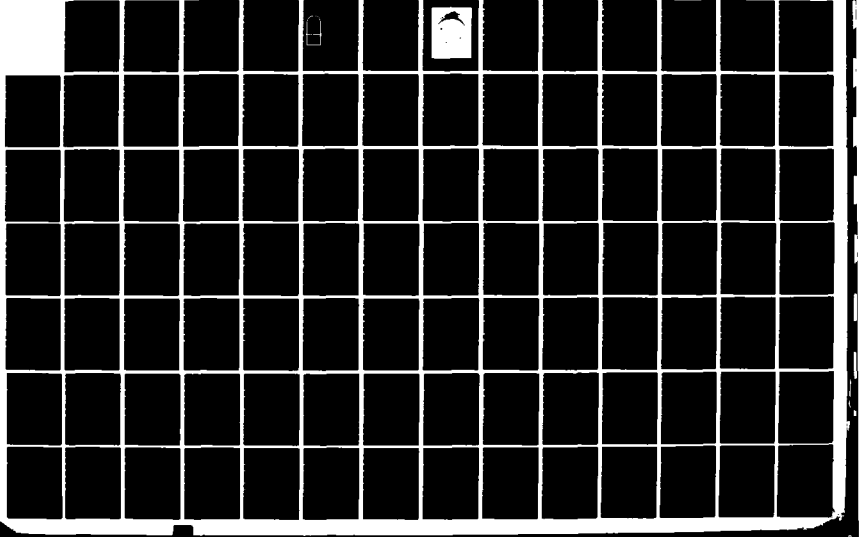

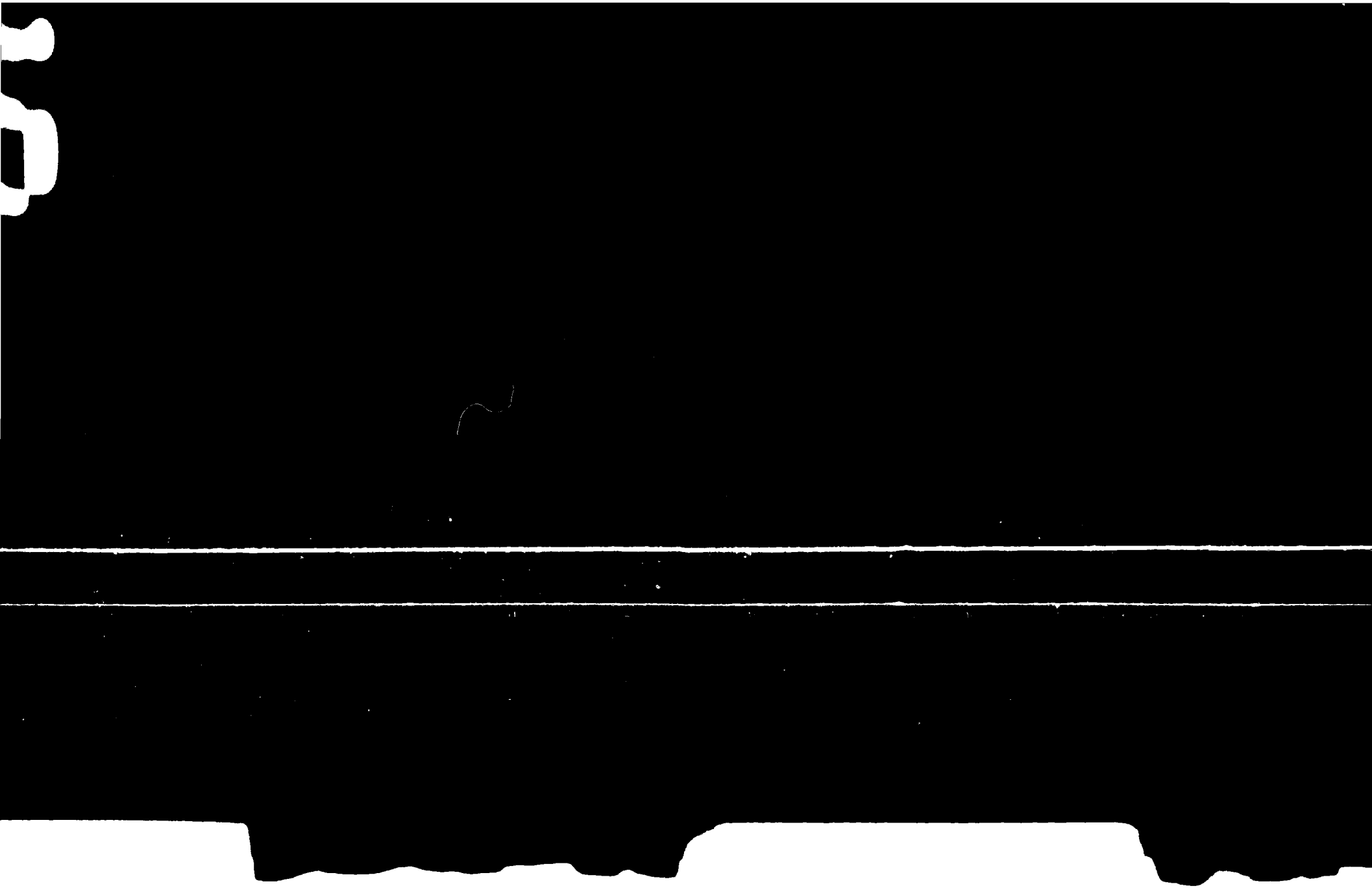

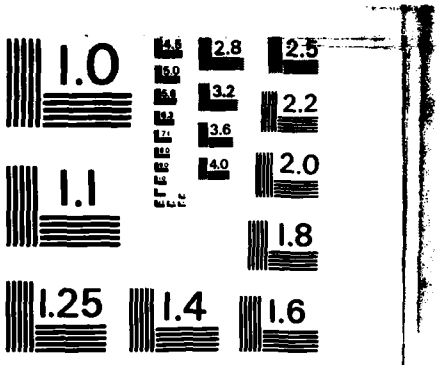

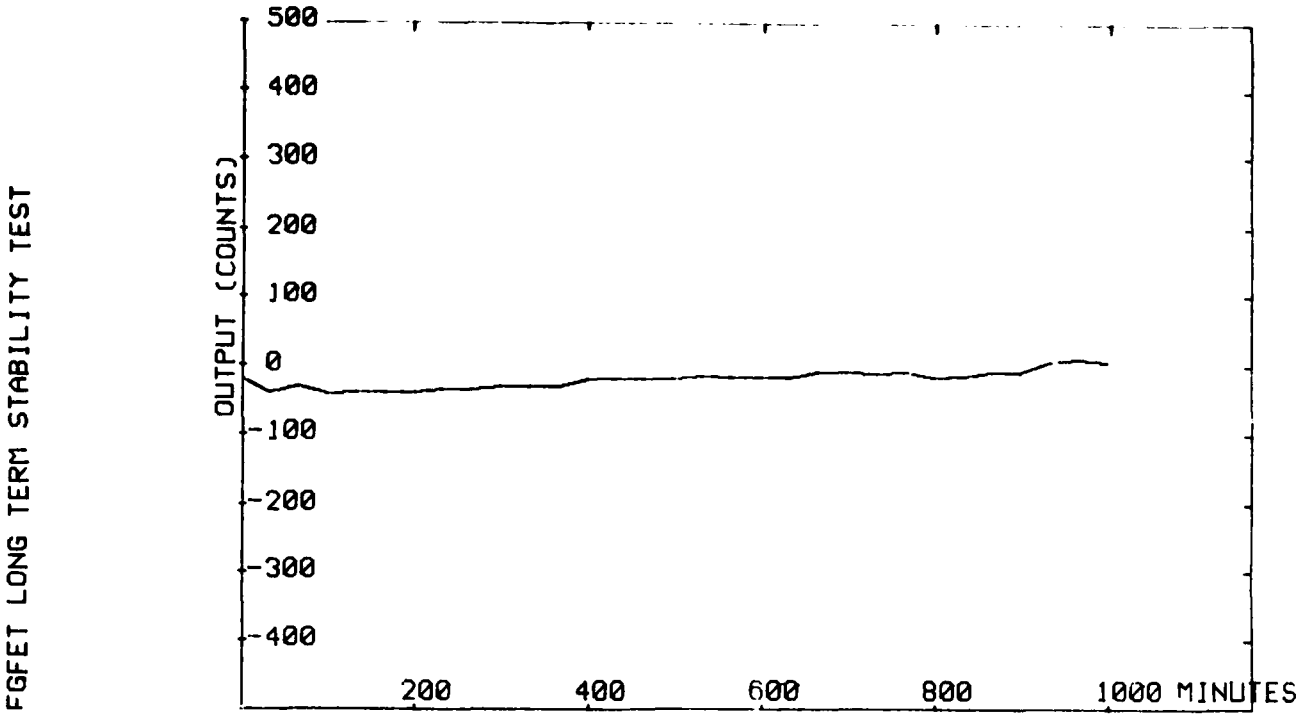

Figure 7.5 Long term stability test on FGFET probe. External field is zero.

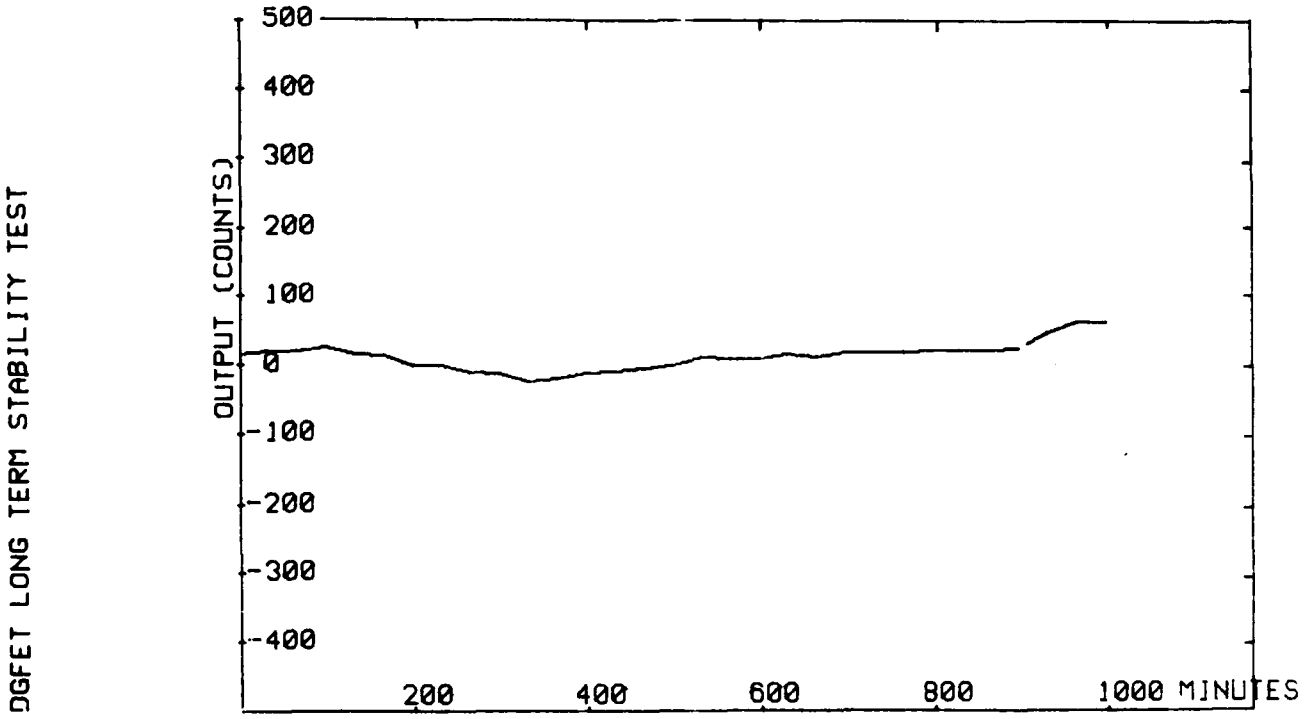

Figure 7.6 Long term stability test on DGFET probe. External field is zero.

is not directly related to the development of gateless sensor, the observations and possible conclusions are of sufficient interest to be included here.

The first arc occured when the FGFET probe was being calibrated. When the high voltage supply was raised above 9 kV, a dip in its output was seen to occur, after which time the synchronous detector went dead. Unfortunately, the exact location of the arc itself was not observed, but it is suspected that arcing occured between the energized plate and the vacuum chamber wall. The gap between these two structures was the shortest in the system and the edges of the energized plate were the sharpest. It is unlikely that arcing occured between the energized plate and the probe head, given the large area of the former, and the large radius of the curvature of the latter.

The second arc occurred when the high voltage was accidentally energized to about 1 kV with the pressure of the vacuum chamber only at rough pump level (about 10^{-3} Torr). Such a pressure level represents the worst possible conditions for sustaining a high voltage gradient, hence, the low arc over voltage is not suprising. It is likely that arcing occurred at the edge of the energized plate in this event also.

In both cases, damage to the probe head and synchronous detector was similiar. Both the sensor and reference op-amp input stages on the sensor interface board were burned out. At the same time, the source leads on both sensor and reference transistors were completely blown off the sensor chip. Note that the reference transistor was completely covered by its outer

case, so that direct contact to the transistor by the arc itself was extremely unlikely.

One possible explanation for the resulting damage requires a description of the properties of vacuum arcs. These arcs generally form so rapidly that the resulting current rises within a few nanoseconds. In the experiments, the vacuum chamber was nominally grounded but it was connected to the chassis of the high voltage supply by a single 1/2" wide braided ground strap, as shown in Figure 7.7. Such a connection, while providing a good dc ground, has an inductance that appears large when compared to a current rise of a few nanoseconds. It is possible, therefore, that during the arcing event, the voltage of the vacuum chamber itself was able to rise significantly above its nominal grounded potential, and the ground potential of the high voltage supply and synchronous detector. (A similar phenomena is observed regularly on electric power transmission line towers that are struck by lightning. Although a given tower is nominally grounded, the inductance present between the top of the tower and the bottom is sufficient to cause the top of the tower to rise to several hundred kilovolts above ground potential).

If such a mechanism were at work on the AFGL vacuum chamber, the observed sensor and circuitry damage could be explained. In the case of the probe head, the source lead of both sensor and reference transitors is kept at quasi- ground potential by the current amplifiers in the input stage of the interface board. Thus if the vacuum chamber and probe head mounted on it rise to a high potential at the instant of arc

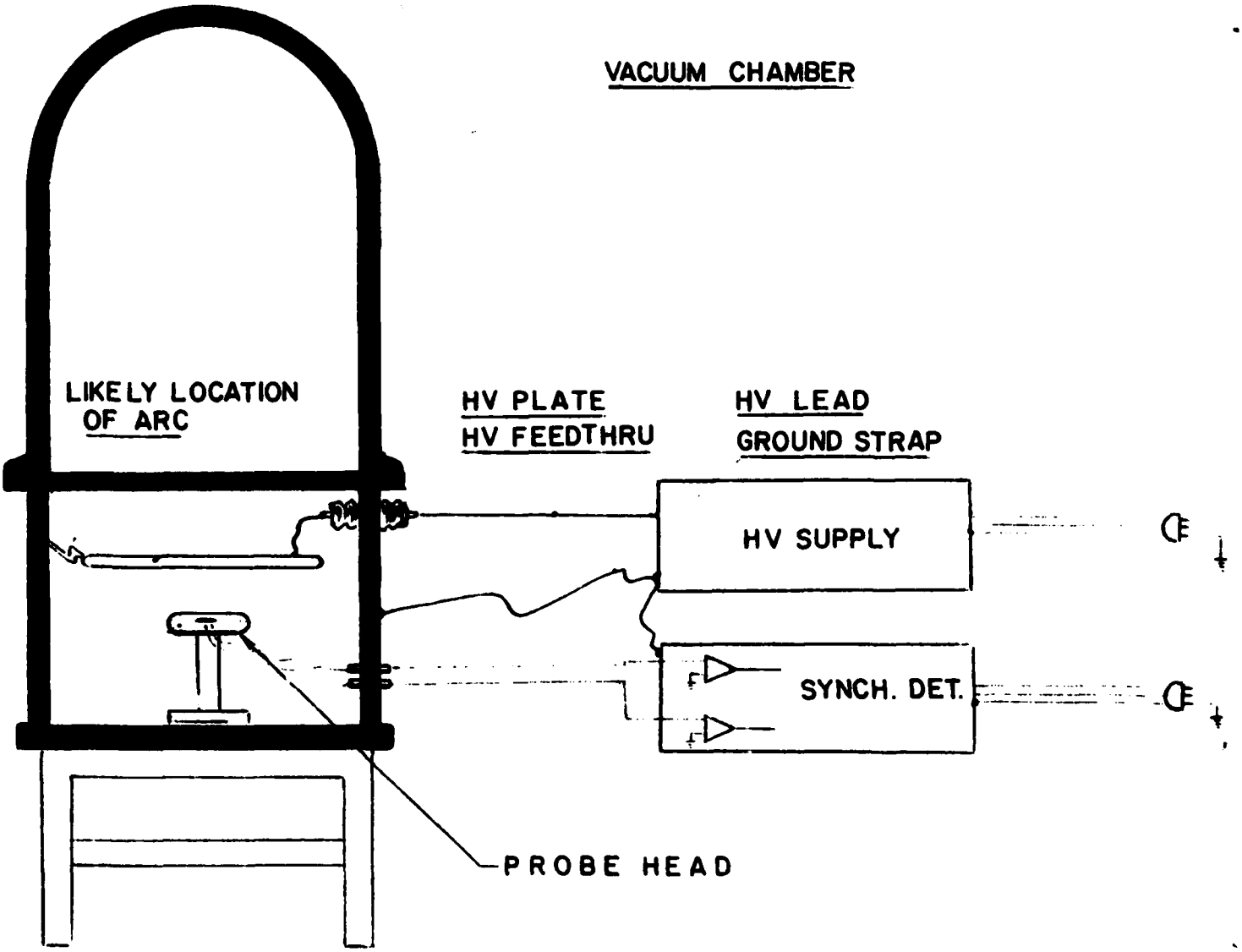

Figure 7.7 Grounding connections between vacuum chamber, synchronous detector, and high voltage supply.

initiation, while the source lead remains at quasi-ground potential, an arc may occur between the substrate of the transistor, which is bonded to the probe head potential, and the transistor source lead. The resulting current flow, even if only a small fraction of the total arc current flowing from power supply to ground through the vacuum chamber walls, could be enough to melt and destroy the very thin bonding wire connecting the transistor source pad to the header pin.

Evidence does exist to support this theory of arc induced damage. Consider, for example the photographs of the damaged sensor and reference transistors taken under a microscope at AFGL (see Figure 7.8). Arc damage is confined to the region around the source bonding pad, which is in fact the outermost electrode structure on the chip face, and thus most readily exposed to the grounded electrode body. Moreover, the position of the damaging arc track can be imagined to have originated at the base of the chip mounting area and to have proceeded up to the source bonding pad.

Although the above explanation is only a hypothesis, it is plausable. With the aid of a high speed transient recorder, it should be possible to conduct further tests, to see if the theory can be corroborated under controlled conditions.

7.5 Plasma Tests

Attempts to run both the FGFET and DGFET probes in the presence of an Argon plasma source. In both cases, the detector

Figure 7.8 Photograph of FGFET damage as a result of vacuum arc.

output saturated when just the filament of the plasma source was energized (with no gas input). Although the FGFET was somewhat less sensitive than the DGFET to this minimal amount of plasma, it does seem that neither device will behave well in such an environment. Such a result is not surprising, given the extreme sensitivity of the devices to the electric fields associated with charges that land on and remain on the floating gate or insulating oxide layer associated with each type of sensor.

7.6 RF Radiation Tests

Attempts were made to run the surface potential probe system in the vicinity of a source of rf radiation. A transmitter operating in the 145 mHz range, with a short "rubber ducky" antenna, and an output of about 100 mW or 1W was situated in close proximity to the measuring instrument. In all cases, the output of the detector was swamped by the presence of the transmitter.

Such behavior was observed even when the FGFET and DGFET transistors were replaced by "dummy" passive resistors. Hence it seems that the design of the synchronous detector itself is susceptible to rf radiation, to such a degree that the assessment of the effects of such radiation on the sensors themselves cannot be made at this time. Such an evaluation can only be made if modifications are made to the synchronous detector box so as to make it "rf tight".

8. CONCLUSIONS

Although the Floating Gate Field Effect Transistor (FGFET) and the Direct gate Field Effect Transistor (DGFET) are still in the early stages of development, it has been shown that both devices are capable of monitoring electrostatic fields and surface potentials. As indicated by the specifications of Table 8.1, which compares the FGFET and DGFET to an unmodified MOSFET, both devices offer improved performance over standard unmodified MOSFETS, in that field readings can be sustained for much longer periods of time. In addition, the danger of MOS related electrostatic damage (ESD) is likely to be less for the FGFET device, and is unlikely to occur at all in the DGFET.

The issue of long term stability may still require further resolution; however, tests in the AFGL vacuum chamber have been encouraging. Many of the long term stability problems encountered when testing the devices in the air seem to dramatically disappear, or decrease in magnitude, when the devices are tested in vacuum. Further evaluation of the stability issue should be reserved until more tests can be conducted on the probes in the AFGL vacuum chamber by AFGL personnel. Work will also continue on an informal basis at the lab at Boston University, so that a definitive decision can be made as to whether or not either sensor is suitable for actual flight use. The general impression one is left with at this point in time is that neither device, using the systems developed so far is reliable enough for such demanding work.

Table 8.1 Comparison of FGFET, DGFET, and MOSFET Electrostatic Field Sensors

Device	FGFET	DGFET	MOSFET
Relaxation Time Constant	1-5 hrs.	15-100 hrs.	10min - 1hr. (in air)
Sensitivity in Δi_D per kV/cm per 1V of V_{DS}	~1.8μA	~0.15μA	
Self Modulation Effect	yes	no	yes
DC Operating point drift		lowest	highest
Susceptibility to ESD damage		lowest	highest
Susceptibility to light and radiation		highest	lowest

It is evident that if the device is to be used at all, thermal control will be necessary. The power requirements of the thermal control system might be considered too large to make the sensor feasible for flight use.

In any event, the experiments can be considered successful. It has been shown that a direct gate sensor will work, and much of the theory surrounding the floating gate sensor has been hypothesized and corroborated with experimental data. It is suggested that any further work be directed towards improving device stability in the face of temperature and extraneous ambient environment changes.

One possible approach would be the fabrication of an integrated sensor on its own integrated circuit chip, whereby sensor, reference, and temperature control components were all located adjacent to each other on the same semiconductor substrate. Yet another approach might involve the incorporation of a multitude of sensors on a VLSI structure, each having slightly different threshold voltages. A digital sampling of which devices were turned on by the field might lead to a drift independent field measurement.

It should be noted that, at present, it is the dc drift problem that presents the most significant drawback in the use of the FGFET and DGFET as field sensors. In certain applications involving the measurement of fast transient fields, these devices may be superior to existing methods. Time resolution of mechanical type sensors is limited to about one vibration period (typically 1 msec or more). The rise times of sensor systems

utilizing FGFET's and DGFET's, on the other hand, will generally be limited by the external circuitry connected to the devices, and not by the devices themselves. While specific rise time tests were not conducted on the FGFET and DGFET sensors, values in the 10-100 nanosecond range can be expected. One possible area for future work might be the evaluation of the high speed performance of the FGFET and DGFET sensors.

The advantage of these devices over capacitively coupled conventional MOSFET (i.e., "electrometer") devices in measuring transient fields may also lie in their reduced susceptibility to ESD damage. (Note that while some FGFET devices sustained arcing damage in the tests reported here, the damage was not of the classic ESD type, and likely was due to causes that would have affected any electronic component, whether or not of the MOS family). Thus another possible area of future work might involve specific comparisons of the ESD susceptibility of MOSFET's, FGFET's, and DGFET's.

9. ACKNOWLEDGEMENTS

The Principal Investigators wish to thank the Air Force Geophysics Laboratory for the support necessary for the conduct of this research contract. In particular, the technical and administrative help provided by Herb Cohen and William Huber were valuable. Gerrard McAndrews offered a great deal of assitance in the performance of the tests in the AFGL vacuum chamber, and Lt. William Kaneshiro assisted as contract monitor in the later phases of the research.

We also wish to thank Dr. Terrence Heng of Unitrode Corporation for his help and assistance in designing and providing the Direct Gate Field Effect Transistors and the Motorola Corporation for its attempt to provide die matched 2N3797 field effect transistors. In particular the efforts of Karin Paoletti, Ray Adams, and Dave Crowder all of Motorola are to be acknowledged.

The efforts of Si Thien Le, who prepared many of the figures, and Donna Zannelli, who helped with manuscript typing, are greatly appreciated.

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APPENDIX A - LIST OF PROJECT PARTICIPANTS

The following personnel participated in various phases of the research project:

Name	Title	Role
Dr. Mark Horenstein	Asst. Professor	Principal Investigator
Dr. Anton Mavretic	Assoc. Professor	Co-Principal Investigator
Edmund Walsh	Master's Degree Candidate	Research Assistant
Robert Desrosiers	Undergraduate	Laboratory Assistant
Si Thien Le	Undergraduate	Laboratory Assistant
Edward Ramsden	Undergraduate	Laboratory Assistant
Angel Rosario	Undergraduate	Laboratory Assistant
Glen Corso	Undergraduate	Laboratory Assistant
Peter Wolniansky	Undergraduate	Laboratory Assistant

APPENDIX B - THEORY OF SYNCHRONOUS DETECTION

A simplified analysis of the synchronous detection system which yields the output of the detector circuit when the FGFET or DGFET sensor is connected at its input, will be offered here. The detector consists basically of a series of two multipliers, followed by a low-pass filter. If the output of the sensor is sampled by a periodic signal, it in effect becomes multiplied by a sinusoid of the same frequency and phase as the synchronous square wave used for sampling. If we now consider this trigononmetric multiplication, we get the following expression for the input to the integrator:

$$x_c(t) = x(t) \cos w_c t.$$

In our case, $w_c = 2\pi$ (1 kHz). If we include random noise, expressed as the frequency components that are both in phase and out of phase with $\cos w_c t$, the input v(t) to the multiplexer becomes:

$$v(t) = [A_1 A_2\ x(t) \cos w_c t] + [n_c(t) \cos w_c t - n_s(t) \sin w_c t]$$

where

$$[n_c(t) \cos w_c t - n_s(t) \sin w_c t]$$

represents narrow band noise, centered around the sampling frequency w_c, that passes through the synch detector. The output of the two-channel multiplexer, which is subsequently fed into the integrator (low-pass filter), is again effectively multiplied by $\cos w_c t$, so that it becomes equal to:

$$e(t) = v(t) \cos w_c t$$

$$= 1/2[A_1A_2x(t) + n_c(t)] +$$

$$1/2[A_1A_2x(t) + n_c(t) \cdot \cos 2w_c t - n_s(t) \cdot \sin 2w_c t],$$

where the relations: $\cos^2 x = 1/2(1 + \cos 2x)$

and $\sin x \cdot \cos x = 1/2 \sin 2x$

have been used.

Note that the only resulting low frequency signals are $A_1A_2x(t)$ and $n_c(t)$, as long as the clock frequency to the multiplexer is exactly in phase with the sampling waveform. (In the expressions above, the time delay caused by the amplifier is cancelled by an equivalent time delay placed before the $\cos w_c t$ input to the multiplexer, and hence is not included in the equations.)

Because the higher order harmonics are filtered out by the low-pass filter, its output will be equal to:

$$V_{OUT} = K_D [A_1A_2 x(t) + n_c(t)]$$

where K_D is the transfer constant of the low-pass filter.

From the above equation, we see that the noise component $n_c(t)$, and the sampled signal that carries the desired information, are additive at the output, but the quadrature noise component $n_s(t)$ is completely rejected. The output-noise power spectrum is thus substantially reduced by the detector.

Note that the low-pass filter is really an integrator which receives the waveform from the synchronous detector, integrates it for a specific amount of time longer than many sampling cycles, and yields an output waveform that is in the form of a ramp. At the end of the specified integration time,

the ramp reaches a level proportional to the E-field incident on the sensor. The integrator is then given a "hold" command for a few milliseconds, during which time its output is fed to an analog-to-digital converter. After A/D conversion, a "reset" signal is fed to the integrator, which discharges its integrating capacitor to zero. A typical reset duration of 1 ms will be sufficient to fully discharge an integrating capacitor of 0.1 uF. After each reset, integration begins again, so that a new data point can be produced.

Appendix C - Operating Instructions for Probe System Using Synchronous Detector

The following sections describe in detail the procedure to be followed when using either the FGFET or DGFET probe heads and synchronous detector box, supplied to AFGL as part of this contract.

C.1 Function of All Controls in Synchronous Detector

FRONT PANEL CONTROLS

OUTPUT : LCD display that indicates detector output range: ± 500 counts. This display operates from a 9 V battery, located on inner chassis board #10, that may require periodic replacement.

SENSOR & REFERENCE JACKS : Connection points for cables from sensor and reference drain and source leads.

GAIN : Sets gain of range amplifier interfacing sensors to synchronous demodulator to values of 1x, 2x, 5x, 10x (@ GAIN SWITCH = 1,2,3,4 respectively).

INTEGRATOR : Sets integrator capacitor to 1.01 μF (INT = A) or 0.16 μF (INT=B).

ON - OFF : Main ac power switch to all circuit boards.

HEATER : In "on" position, allows power to flow to heater inside probe head, if called for by thermal controller.

In "off" position, no power may flow to heater, and thermal control is effectively disabled.

OUTPUT : (switch) Applies power to LCD "OUTPUT" display (BNC jack). A voltage proportional to surface potential appears here. Maximum value approximately ± 0.5 volts, corresponding to LCD reading of ± 500 counts.

PROBE : This multipin socket interfaces the temperature sensor and heater inside the probe head to the thermal controller board located inside the synchronous detector. (See Fig 6.5):

Pin 1: Heater
Pin 2: Heater
Pin 3: White]
Pin 4: Red] >Connections to Temp Sensor
Pin 5: Black]
Pin 9: Circuit Ground

BALANCE : This BNC jack is connected to the output of the preamplifier circuit that interfaces the sensor and reference to the synchronous detector (see Figure 6.5). Its purpose is to aid in balancing (i.e., zeroing) the sync detector. With no surface potential applied to the probe head, the square wave appearing at this terminal should be set to its minimum peak-to-peak value via the balance switches inside the sync detector, as outlined in Section C.3.

ZERO : Fine tunes balance control switch settings. Clockwise = more negative.

SYNC OUT : Provides a 0-5 volt square wave, synchronized to the sync detector chopping signal of about 400 Hz.

INNER CHASSIS CONTROLS (Located behind front panel cover)

BATTERY : (Board 10) Operates Front Panel LCD display.

BALANCE : (Board 8) Coarse setting for balancing signals from SWITCHES reference and sensor (i.e., zeroing instrument) with no external surface potential applied. Only one of the switches should be in the "ON" (down) position at any given time. To make the output go more negative, select a switch closer to the front of the instrument.

EXCITATION : (Board 8) Row of 10 switches which select the peak-to-peak excitation applied to sensor and reference according to following formula $V_{p-p} = 20/(2^n)$ volts, where n = switch number. Example: 8^{th} switch applies a square wave of $20/(2^8) \cong 80$ mV p-p.

TEMP SET : (Temperature Control Board, located on far left of chassis). Adjusts set point temperature of thermal controller. Clockwise = raise temperature.

V_{SET} : (Temperature Control board) Voltage corresponding to desired output of probe head temperature sensor, and adjusted by TEMP SET control, appears at this terminal relative to chassis ground. Room Temp = 3.35 volts. Raise approx 12mV per ^{o}C above room temperature.

V_{TEMP} : (Temperature Control board) Actual output of temperature sensor on probe head appears at this terminal relative to chassis ground. Ideally, V_{TEMP} will be equal to V_{SET} when thermal controller is at work; In practice, may be lower than V_{SET} by as much as 80 mV. However, its value should be steady in equilibrium (after several minutes thermal warm up).

Room temp ~ 3.35 volts; Slope $\tilde{=}$ 0.08^{o}C/mV

ZERO : (Board 10) Ten turn pot, located on upper edge of ouput display board #10, accessed from <u>top</u> of cabinet, which zeroes center of OUTPUT range. Should be set so that positive and negative maximum scale limits are of equal magnitude.

All other switches and controls inside the sync detector box are not changed during normal operation of the instrument, and hence are not discussed here. Refer to Appendix D for a more detailed discussion.

C.2 Setting Up the Probe System

Either the FGFET or DGFET probe head may be selected for making surface potential measurements. If the FGFET probe is used, the protective TO-18 cover should be removed from the sensor device (See Figures 6.1 and 6.2). If the DGFET probe is used, the plastic protective cover should be removed. The probe head should be mounted so that the top of its toroidal surface is located exactly 5 cm from the surface to be monitored. Deviations from the 5 cm distance will alter overall system calibration in an approximately proportional way. The base plate (see Fig. 6.1) is normally used when the probe torus is to be held in a horizontal position. If desired, however, this base plate may be removed, and the probe head mounted in another position via the tapped 1/4"-20 mounting hole at the bottom of the support cyllinder. To preserve probe calibration, this 1" diameter support cyllinder should always be used to mount the probe head, so that the same approximate probe geometry used to calibrate the system is maintained.

The coaxial cables leading to the reference and the sensor should next be connected to their appropriate sockets on the synchronous detector instrument panel (See Figure C.1). The sensor cable is differentiated from the reference cable by being marked at the end with a white dot. The center conductors from each coaxial cable are connected to the drain terminals marked "D", and the outer shield conductors are connected to the source terminals marked "S". Note that although these outer shields are at ground potential, they do carry signal currents, and

should by insulated from chassis ground. If the coaxial cables are passed through a vacuum feedthrough flange, for example, separate insulated terminals must be allocated to the outer shields. Chassis, or circuit ground between the probe head and the synchronous detector is automatically made by pin #9 in the multiconductor temperature controller cable.

Final connection of the probe head should be via the multipin cable that interfaces the thermal control system to the temperature sensor and heater inside the probe head. Note that if thermal control is <u>not</u> desired, this cable connection may be omitted, provided that a separate ground connection is made from the probe head at the base of the torus back to a convenient chassis ground on the synchronous detector. Should penetration through a vacuum flange be required, it is best to insulate this chassis ground from vacuum chamber ground to help minimize noise from ground loops.

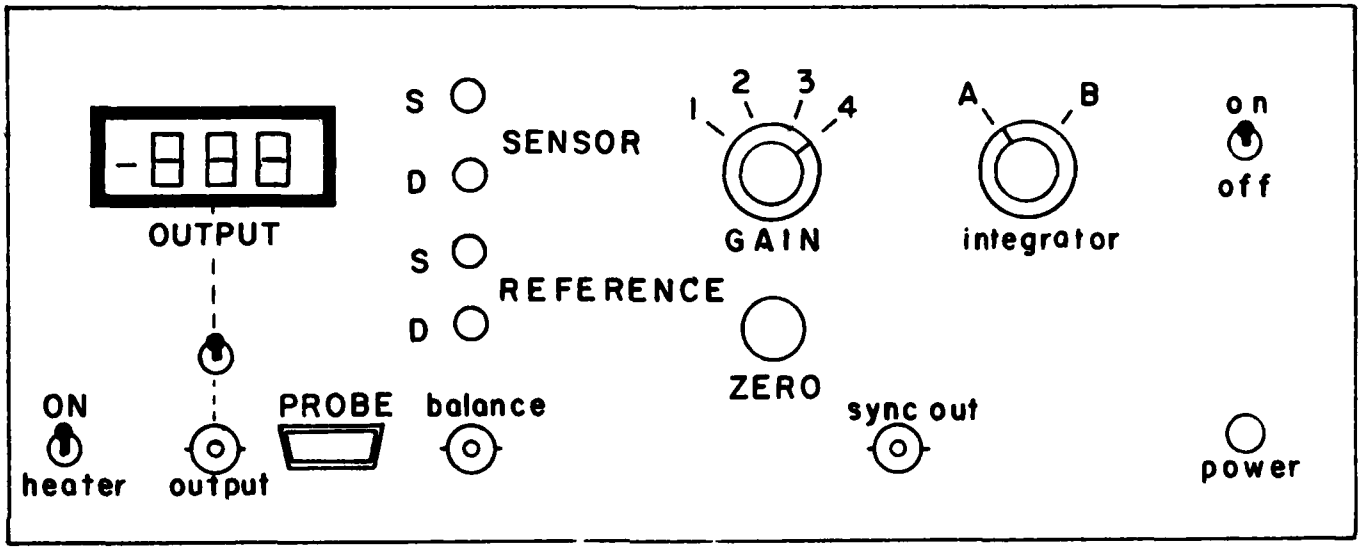

Figure C.1 Front Panel of Synchronous Detector

C.3 Monitoring Instruments

As an aid to initial calibration or setup, it is helpful to connect several diagnostic instruments as follows:

OSCILLOSCOPE: Connect an oscilloscope to the BALANCE output to aid in balancing the instrument.

TEMPERATURE METERS : Connect a digital meter differentially across the V_{SET} and V_{TEMP} terminals (Positive lead to V_{SET}, negative lead to V_{TEMP}). This meter will thus read the difference between V_{SET} and V_{TEMP}, which should normally have a positive value on the order of 100 mV or less.

OUTPUT METER: Because it is difficult to view the OUTPUT LCD when the front panel cover is open, it may be helpful to connect an external display meter, set to read voltages up to $\pm$ 0.5V, to the OUTPUT terminal.

C.4 Balancing Procedure

With the probe head properly installed as described in Section C.2, and the vacuum system pumped down if operating in vacuum, the switches located inside the synchronous detector box should be set according to the following procedure:

1. Select the desired excitation and Gain settings for the probe head being used. Normally, these settings should be as follows:

FGFET probe:
Ex Switch #8 (inner chassis)
GAIN Switch #3 (front panel)
INTEGRATOR = A (left position)(front panel)

DGFET probe:
Ex Switch #6
GAIN Switch #4
INTEGRATOR = A

With these excitation and gain settings, the instrument will be

calibrated according to Figures C.2 and C.3.

2. Energize the thermal controller by turning the heater ON. After several minutes warm up, the V_{TEMP} level should approach the V_{SET} level (as indicated by the diagnostic meter described in Section C.3, if installed) to within 100mV. Under most conditions ten minutes should be more than sufficient time for the thermal system to reach equilibrium.

When the thermal controller has stabilized, the instrument is ready to be balanced. With no external surface potential applied to the probe:

3. Set all BALANCE Switches to the OFF (up) position (eight switches in all, located on inner chassis)

Turn ZERO control fully clockwise (most negative position)

The OUTPUT display reading should be at negative maximum scale limit.

4. One by one, beginning with BALANCE Switch #1 (switch closest to front of cabinet) push single BALANCE switches to the ON position and observe OUTPUT. If OUTPUT remains negative, return given switch to the OFF position, and go on to the next switch. When the switch is identified that makes output go positive, return it to the OFF position, back up one switch, and leave preceeding switch in ON position. An oscilloscope connected to the BALANCE output on the front panel may be helpful in this step. Minimum peak-to-peak square wave is desired.

When Step 4 is completed, only one BALANCE switch should be in the ON position. Typical settings might be:

FGFET probe: BAL Switch #6
DGFET probe: BAL Switch #6

Note that the setting of the BALANCE switches does not affect instrument calibration.

5. Turn the ZERO control (front panel) counterclockwise until the OUTPUT reading equals zero.

The instrument is now balanced, and ready to measure surface potential. Occasional adjustment of the front panel ZERO control may be necessary to compensate for temperature and bias drifts in the sensor and reference.

If the probe head is changed the GAIN and EXCITATION settings should be changed and the balanceprocedure (Steps 3-5) repeated.

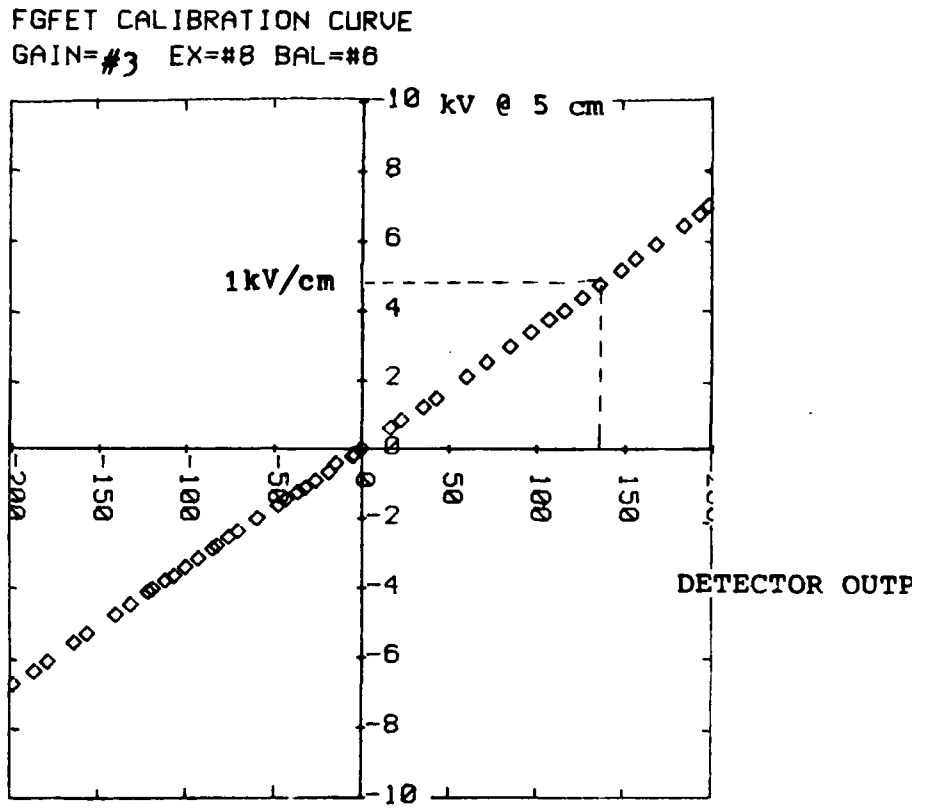

Figure C.2 FGFET Probe calibration curve @ 5 cm

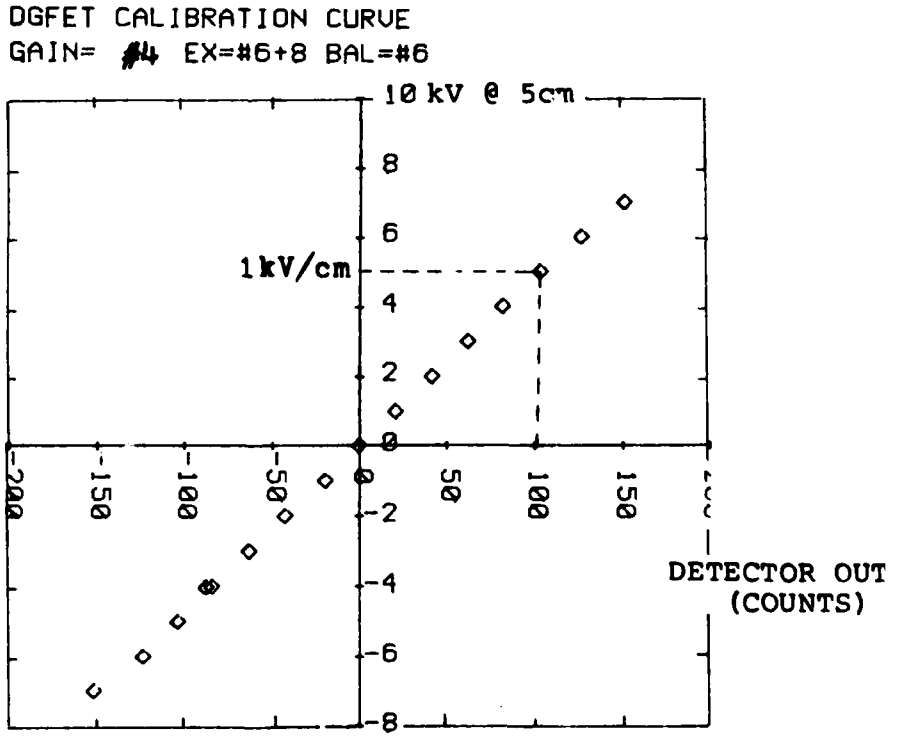

Figure C.3 DGFET probe calibration curve @ 5 cm

Appendix D - Description of Synchronous Detector Instrument

The synchronous detector system, discussed theoretically in Appendix B, allows extremely low signal levels to be detected, provided that the signal to be detected is "chopped", or synchronized, to the master clock signal generated within the system logic. In the case of the FGFET and DGFET probes, this "chopping" is performed on the sensor interface board by using an ac square wave for the driving signal that biases the sensor and reference transistors, as described in Section 6. The preprocessed signal from the sensor interface board thus consists of a square wave signal whose amplitude is proportional to the electric field or surface potential being measured, plus asynchronous noise picked up by the sensors. It is this signal that is fed to the various stages of the synchronous detector system. Figure D.0 shows a view of the synchronous detector front panel, with the position of all controls.

In all the descriptions that follow, the "Z" locations refer to labeled block locations on the plug in wire wrap boards of the synchronous detector instrument.

D.1 Range Amplifier

The first stage of the synchronous detector is the "range amplifier" section, which further amplifies the signal received from the sensor interface board. The range amplifier (Board No. 5), shown in Figure D.1, consists of three op-amp circuits built around locations Z55 and Z51 (dual op-amp). Most of the resistors used to construct the range amplifier are of the high precision

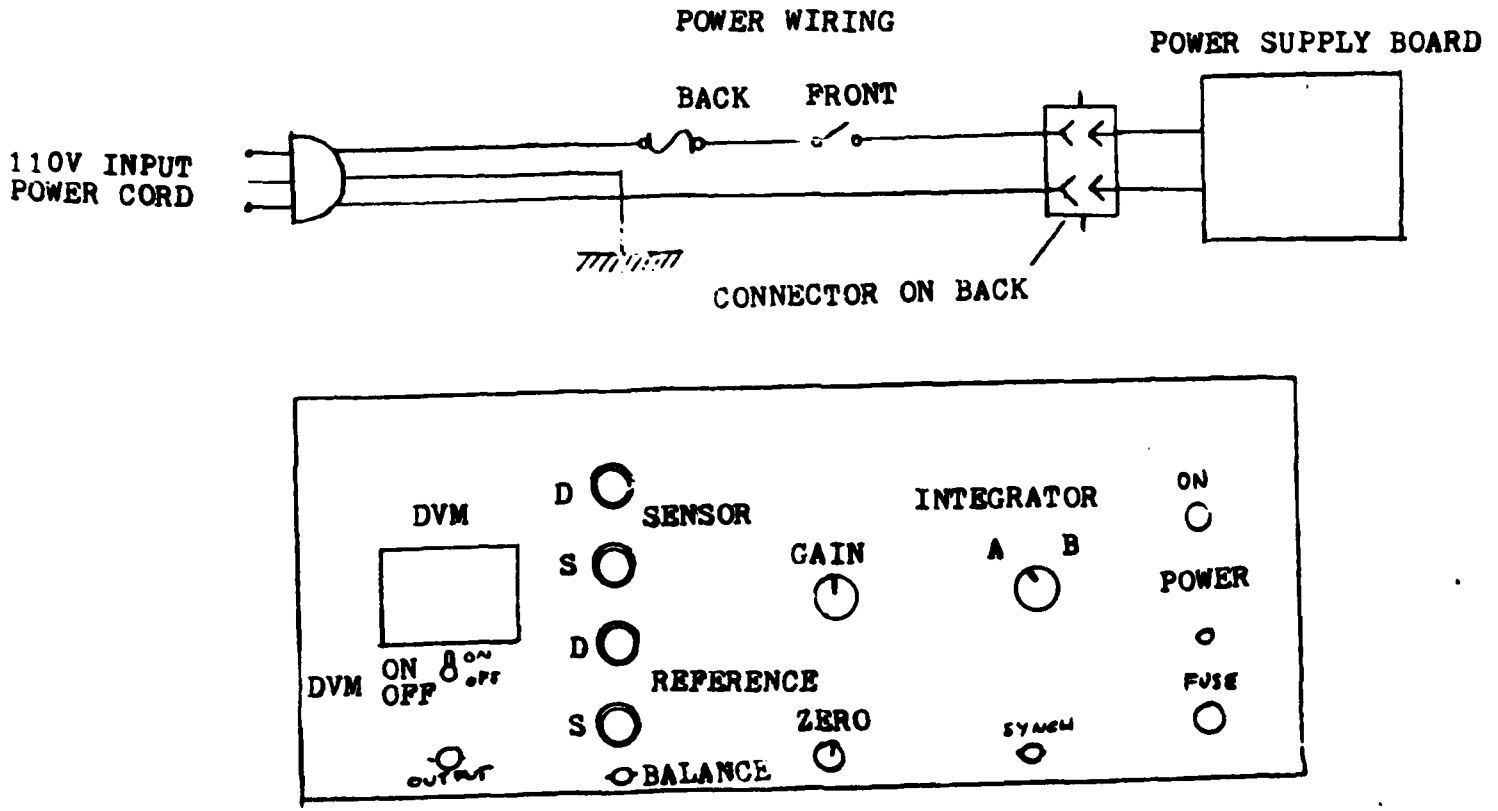

Figure D.0 Front Panel of Synchronous Detector

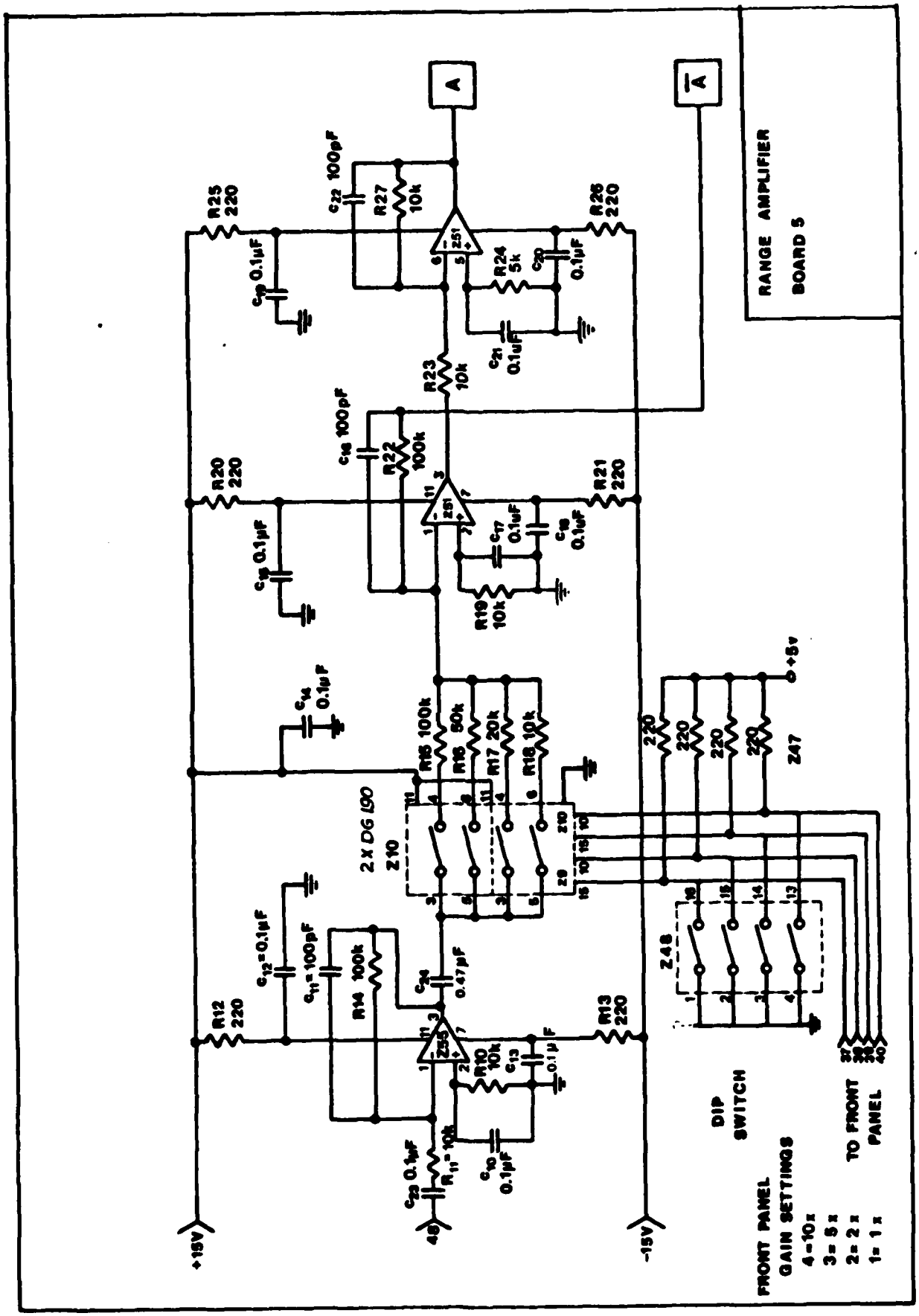

Figure D.1 Range Amplifier Board.

DIP type.

Second stage gain selection is accomplished by remote switching of input resistances R15 - R18 to amplifier Z51. These resistors are interfaced to the front panel gain selection switch by two digitally encoded analog multiplexer circuits DG190, located at Z9 and Z10. The DIP switches in location Z48, which are included for testing and debugging purposes, should be kept in the open position, so that logical switch settings from the front panel switch can be received by the DG190 circuits.

The second stage amplifier gain settings available via the front panel rotary switch are 1X, 2X, 5X, and 10X, so that the overall amplifier gains available, given the first stage gain of 10, are 10X, 20X, 50X, and 100X. The outputs of range amplifier are found at points A and $\bar{A}$, where $\bar{A}$ is the inverted version of A.

The output of the range amplifier A and its complement $\bar{A}$ are fed directly to the input of the synch detector circuit, where the actual detection process begins. To minimize lengthy connection paths, the range amplifier circuits are physically located on the same board as the synch detector and integrator circuits.

D.2 Synchronous Detector and Integrator

The synchronous detector and integrator circuits, shown in Figure D.2, are physically located adjacent to one another on the same circuit board as the range amplifier, so that extraneous signals from ground loops, stray pickup, and random noise are minimized.

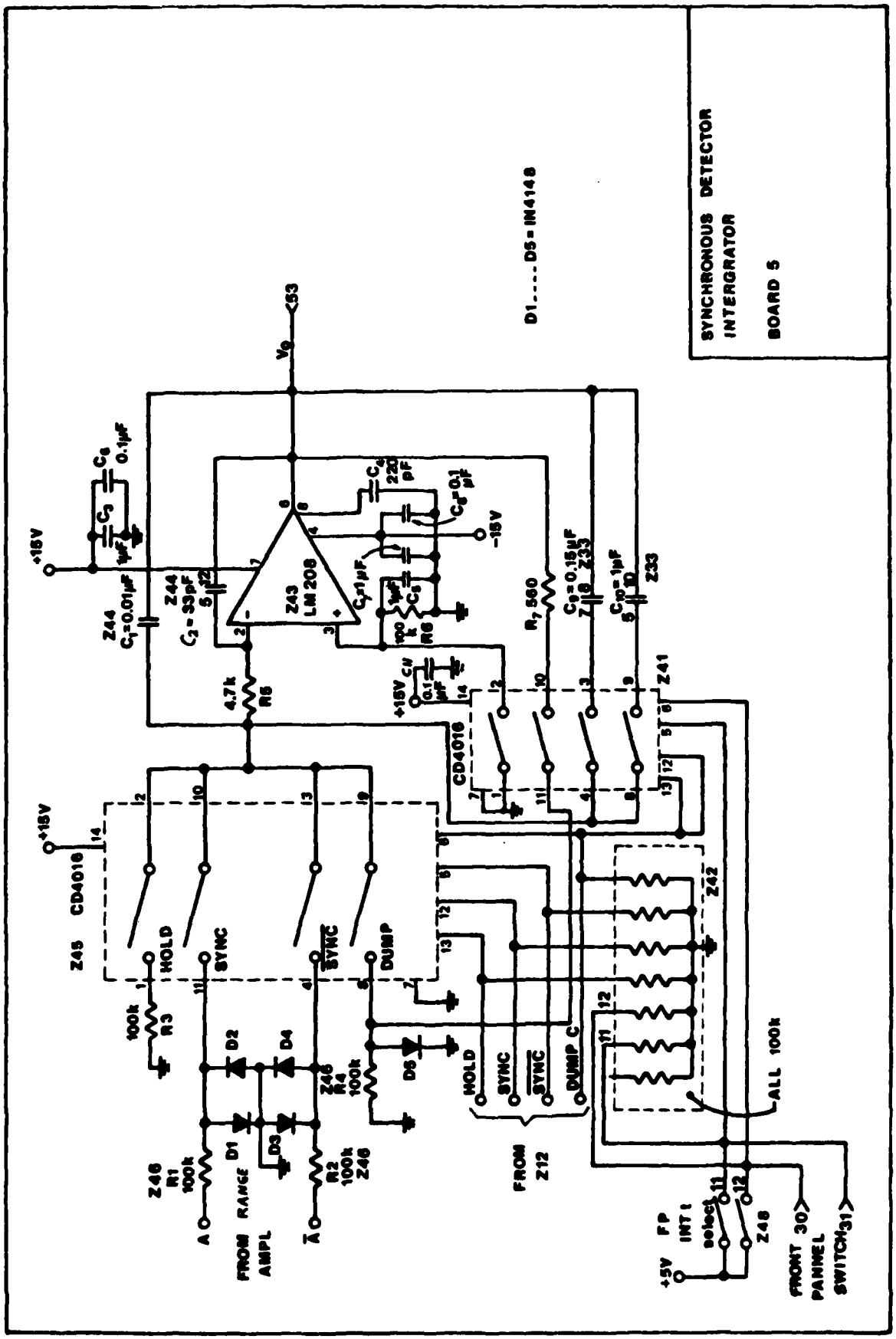

Figure D.2 Synchronous Detector and Intergrator Board.

The core of the synchronous detector is the analog MUX CD4016, located at Z45. The 400 Hz sampling frequency which drives this MUX is derived from the synch generator section, and consists of logic signals SYNC and **SYNC**. During each "synch" interval (SYNC signal high), which lasts for about 1.25 ms, or half the period of the 400 Hz synchronizing frequency, the primary output A of the range amplifier is sampled, while during each "not-synch" interval (**SYNC** signal high), the complementary output **A** of the range amplifier is sampled. The synchronous detector thus alternately samples the positive (+) and negative (-) portions of the incoming signal, behaving somewhat like a full wave rectifier, but preserving the polarity of the input signal.

The output of the CD4016 MUX at Z45 is thus a rectified waveform which is then fed directly into a standard op-amp integrator configuration built around an LM208 amplifier, located at Z43. This particular op-amp was selected because of its low voltage offset and input current bias, and is externally compensated so that it is able to drive the large capacitances of the integrator circuit.

One of the two available integrator capacitors is selected by another DG190 analog MUX, located at Z41. These selectable capacitors are connected in parallel with a fixed 0.01 uF capacitor C_1. The two switched capacitors are C_9 = 0.15 uF and C_{10} = 1 uF. The change in integration capacitances is achieved by logic switching at the front panel rotary switch.

The portion of integration time constant contributed by the fixed, hard wired capacitor C_1, is given by $T_i = R_1C_1 = 10^5 \times 0.01 \times 10^{-6} = 1$ms. Proportional integration times result if C_9 or C_{10} are switched in separately. If both capacitors C_9 and C_{10} are switched in, then the total integration time

constant becomes $T_i = 10^5 \times 1.16 \times 10^{-6} = 116$ ms.

The total time over which integration is allowed to occur is variable, and is selected by a set of binary DIP switches, located at Z17 on the Synch Generator board, Fig D.3. The integration time can be set within the range 20 mS to about 2 seconds, with switch settings for some selected integration times listed in the table included with Fig. D.3. Note that the longer the integration time, the better the signal to noise ratio achievable by the synchronous detector system.

D.3 Logic Control Signals

The logic signals needed to drive the integrator and synchronous detector stages, HOLD, SYNC, SYNC AND DUMP, are generated on the Synch Generator board (Fig D.3). A hold interval is generated immediately after the end of each integration period. During this hold cycle, the analog to digital converter (A/D) converts the sampled output of the integrator to a ten bit digital signal. Holding persists for about 1.25 ms, after which time the integrator is "dumped", i.e. all capacitors are discharged to zero through the 560 Ohm R_7, shown on the Integrator Board, Fig. D.2. Immediately after dumping, the integration period is repeated, thus restarting the entire cycle.

D.4 Clock Generator Circuit

The timing system of the synchronous detector is controlled by the clock generator, shown in Fig. D.4. This clock generator is driven by a 1.024 MHz master crystal oscillator, located at Z36. This clock signal is fed into Z37, which, in combination with Z38, forms a modulo-N counter, which is programmed

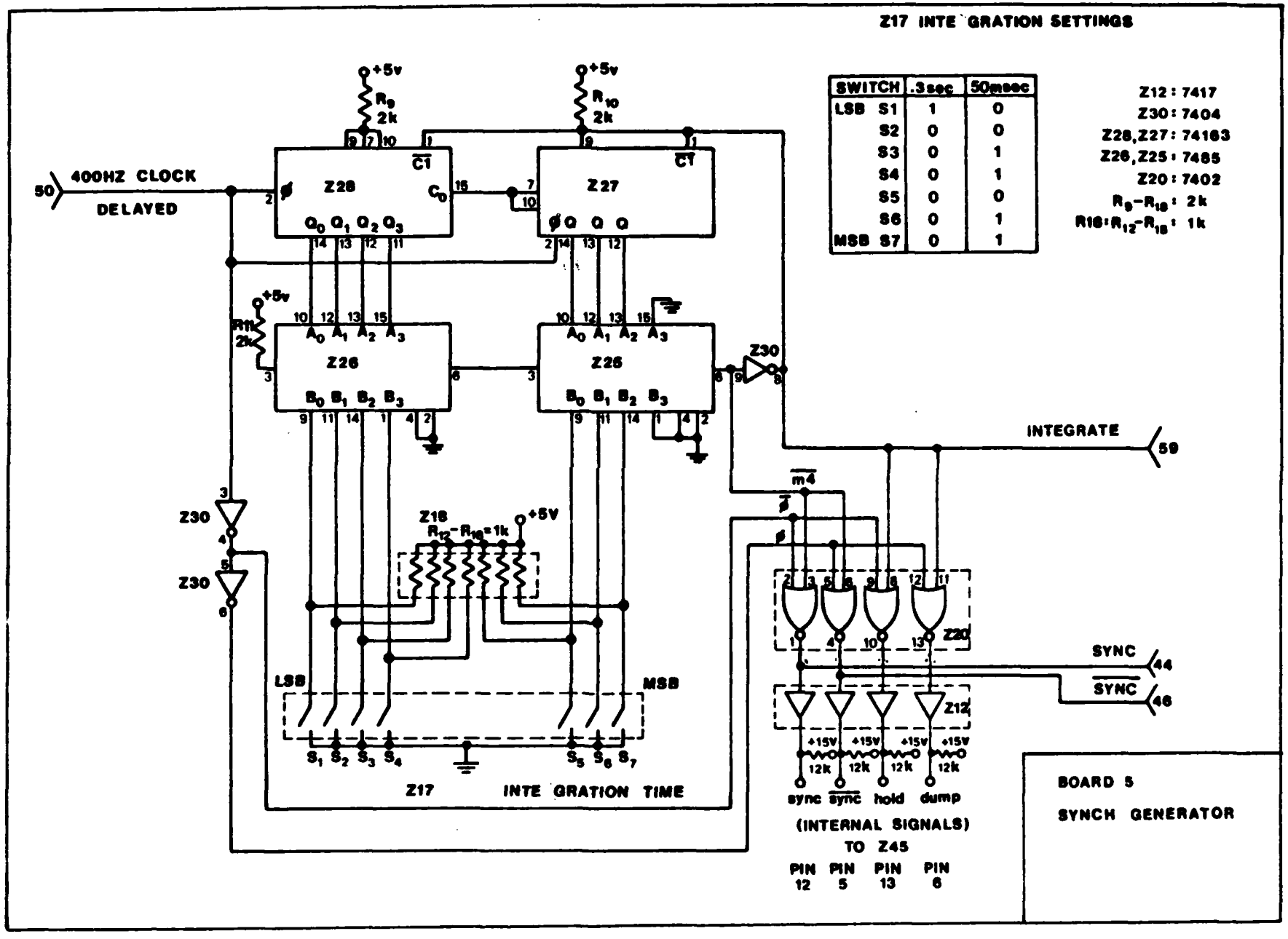

Figure D.3 Synch Generator Board.

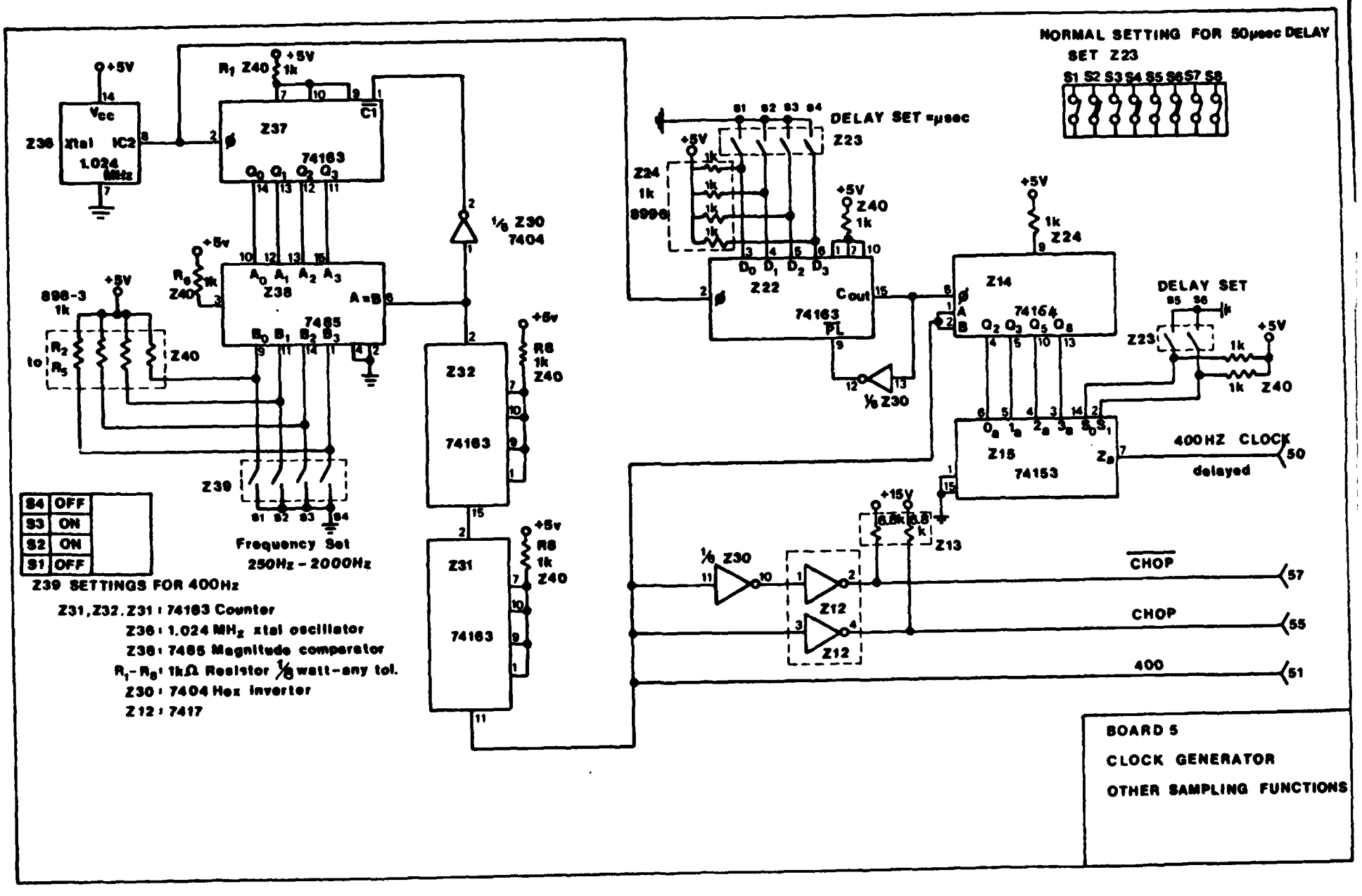

Figure D.4 Clock Generator Board.

through S1-S4 on Z39. The functions of Z31 and Z32 are to divide down the pulse signal from Z38, which has a duration of somewhat less than a microsecond, by a factor of 256, and to provide a 50% duty cycle 400 Hz square wave to the stages that follow.

This 50% duty cycle 400 Hz signal, available at pin (51), is sent to the sensor interface board after being converted into the SYNC and **SYNC** signals, which are 0-15 volt square waves (the level necessary to drive the CD4016 cmos gate) by the buffer amplifiers located on the Synch Generator board (Fig. D.3) at Z12. The SYNC and **SYNC** signals are also avaiable on the backplane of the synchronous detector instrument at pins (44) and (46) for trouble-shooting and expansion purposes.

The divided down signal is also sent to the delay unit on the clock generator board (Z22, Z14, and Z15), where it is delayed by an integral number of master clock periods (0.977 μs), as determined by the switch settings of Z23. Note that not all integral delays are available. Rather, those which can be obtained are in the form of 2k, 3k, 5k, and 8k, where k is an integer from 1 to 15. The resulting delayed signal is used to provide the synchronization to the analog switch network in the integrator. The synchronous detector logic drive is delayed due to the phase shifting that occurs when the analog signal passes through the range amplifier.

D.6 A/D Converter and Sample/Hold

This unit, which is mounted on a separate board (Fig. D.5), performs the functions of A/D conversion and S/H on the output of integrator. The first

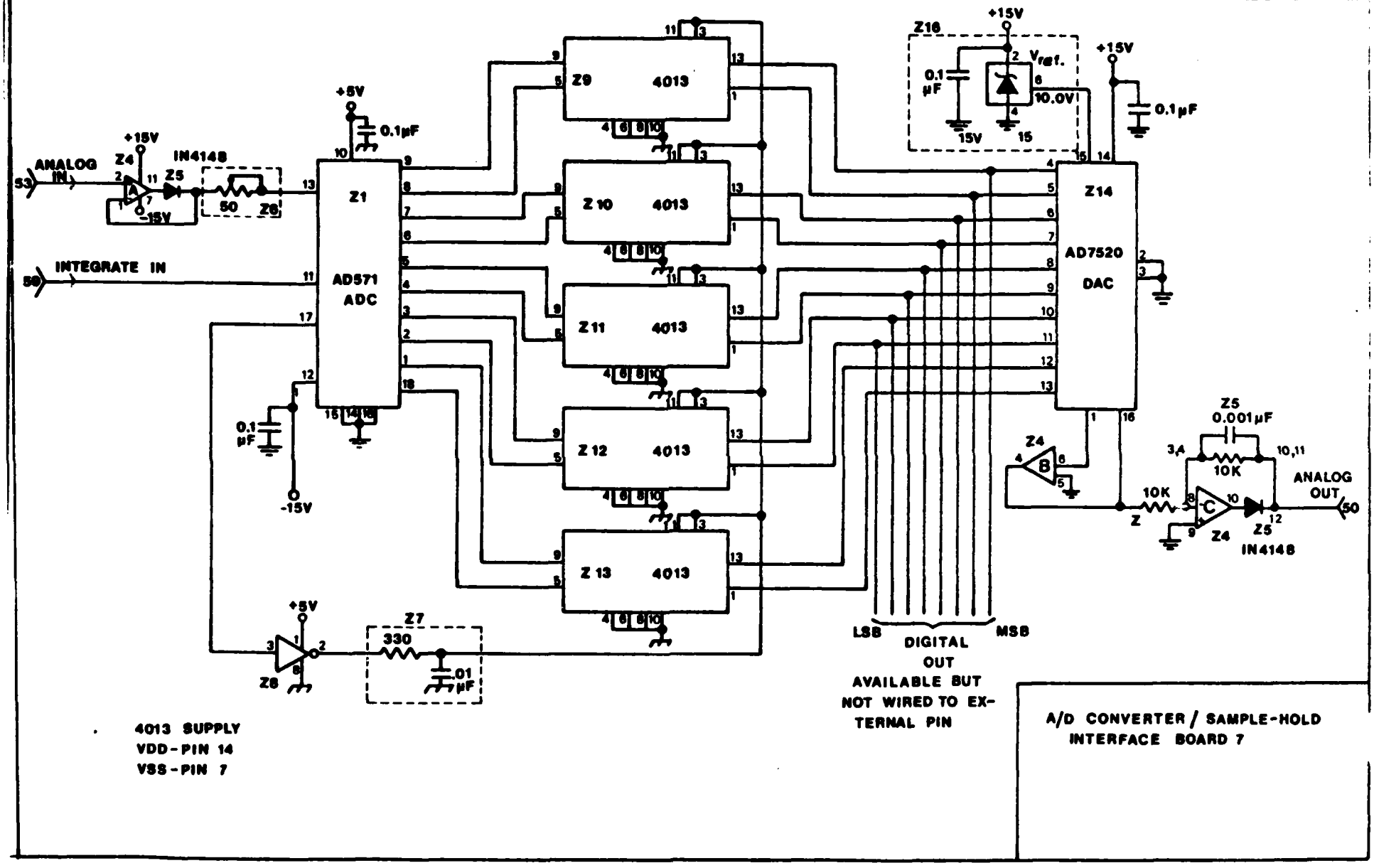

Figure D.5 A/D Converter/ Sample Hold Board.

component section is located at Z1, which performs the convert function as well as the trim/clamp function, on the analog output of the integrator. The device is started by the negative edge of the integrate signal, and produces a ten bit digital word which is latched into the banl of CD4013 D-flipflops.

At this point, the output of the integrator, which is in essence the output of the synchronous detector systen, is available as a digital number (although not at present connected to any external pins), which is then converted back to an analog voltage for input to the front panel meter.

D.6. Timing Diagram

A summary of all signal timing events is shown in Fig. D.6.

D.7 Wiring Diagrams

The backplane wiring diagrams for each of the boards discussed above are shown in Figs. D.7 through D.10, while the front and back slot locations for each board are given in Figs. D.11 and D.12.

Front panel switch color coding is given in Fig. D.13.

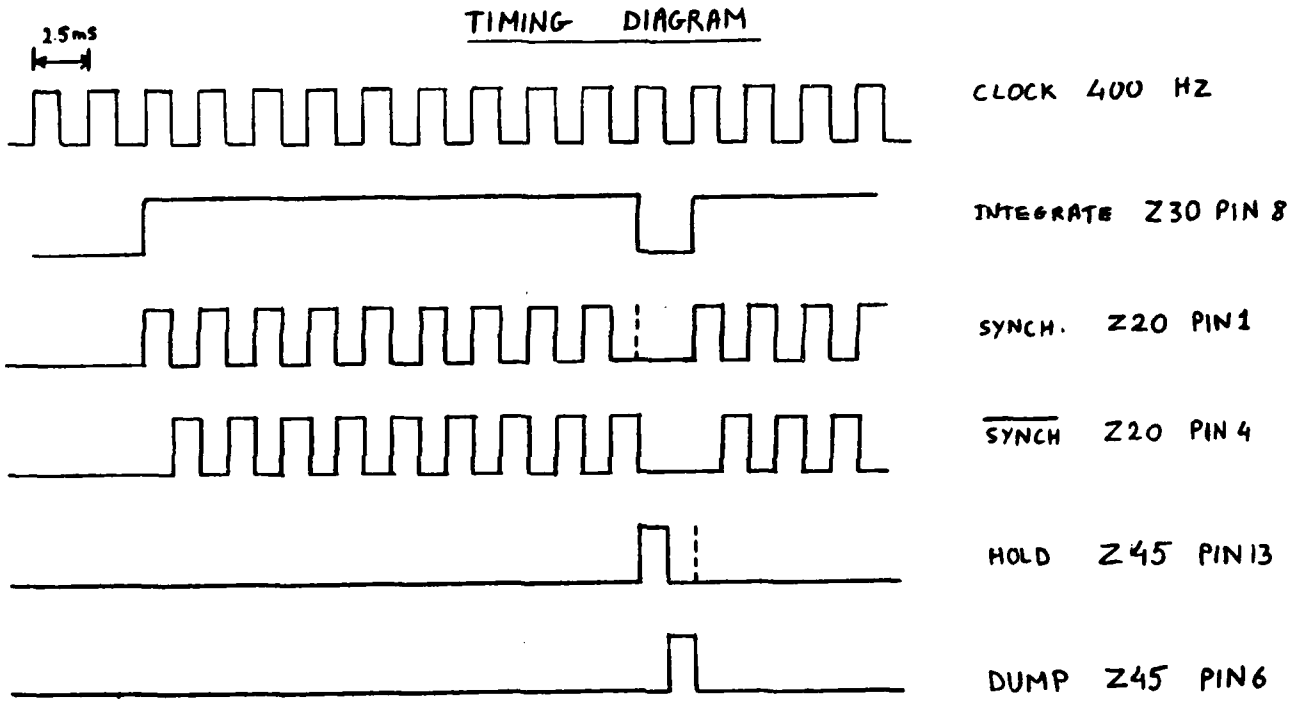

Figure D.6 System Timing Diagram

Figure D.7

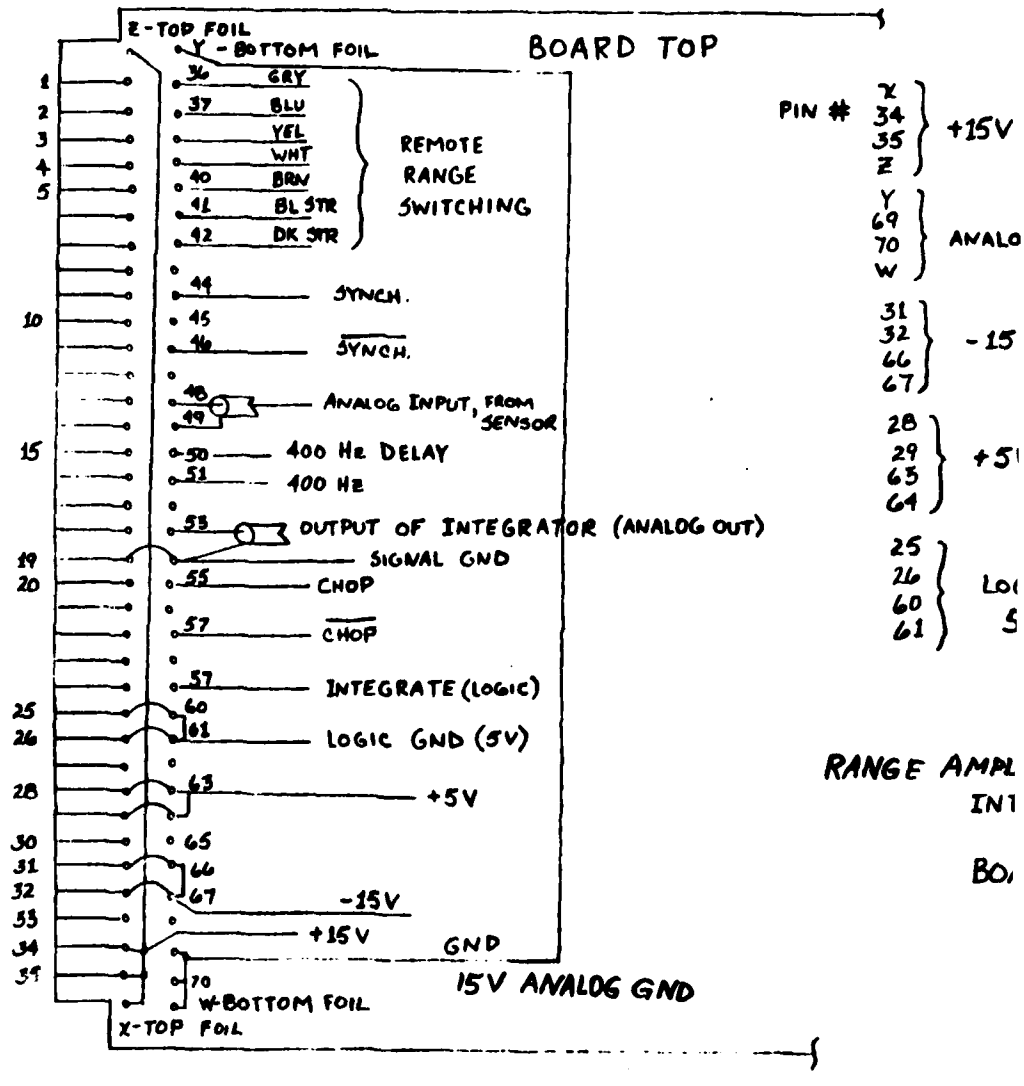

Figure D.7

Back Plane Wiring Diagram for Range Amplifier and Synchronous Detector Board.

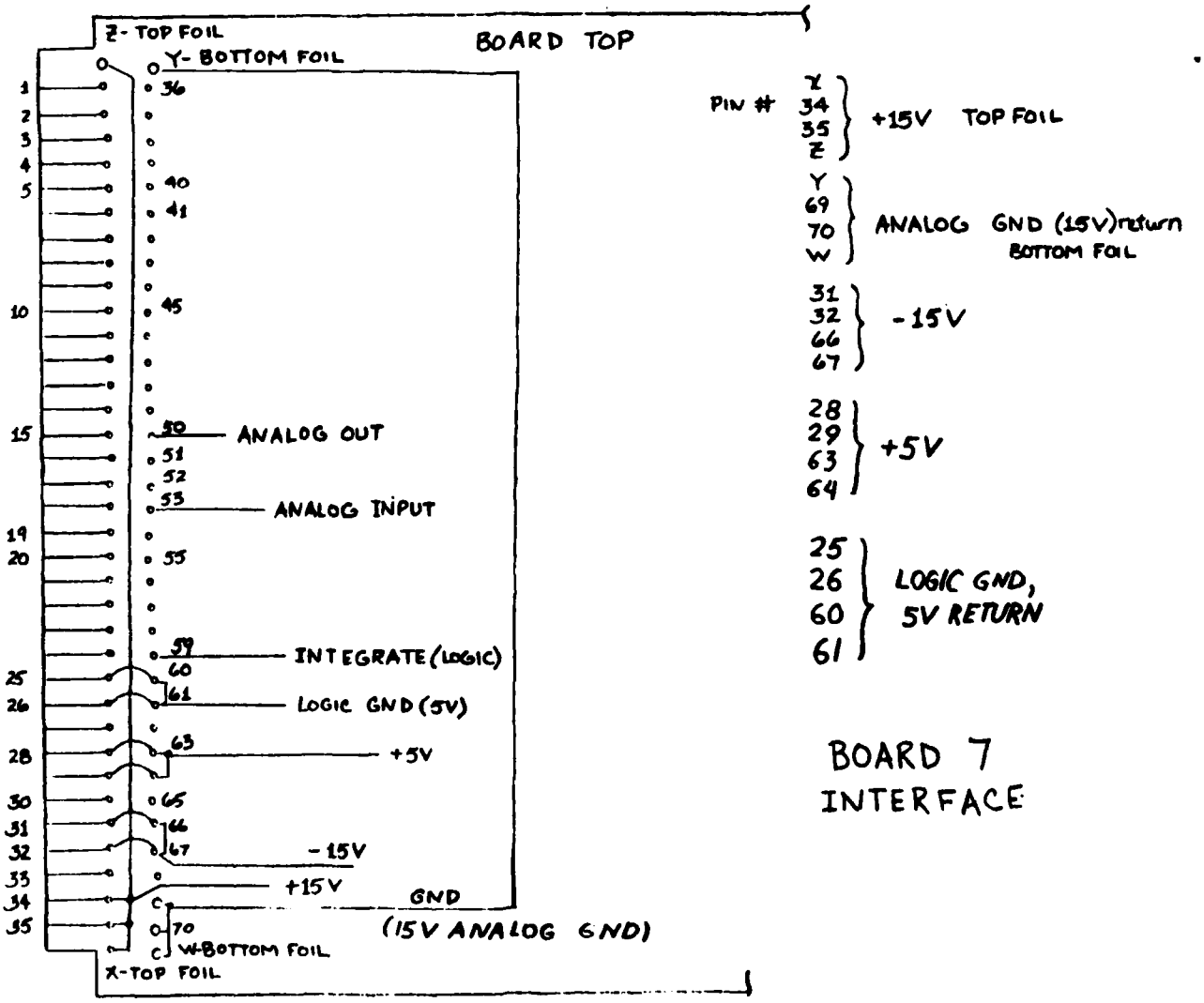

Figure D.8 Back Plane Wiring Diagram for Interface Board.

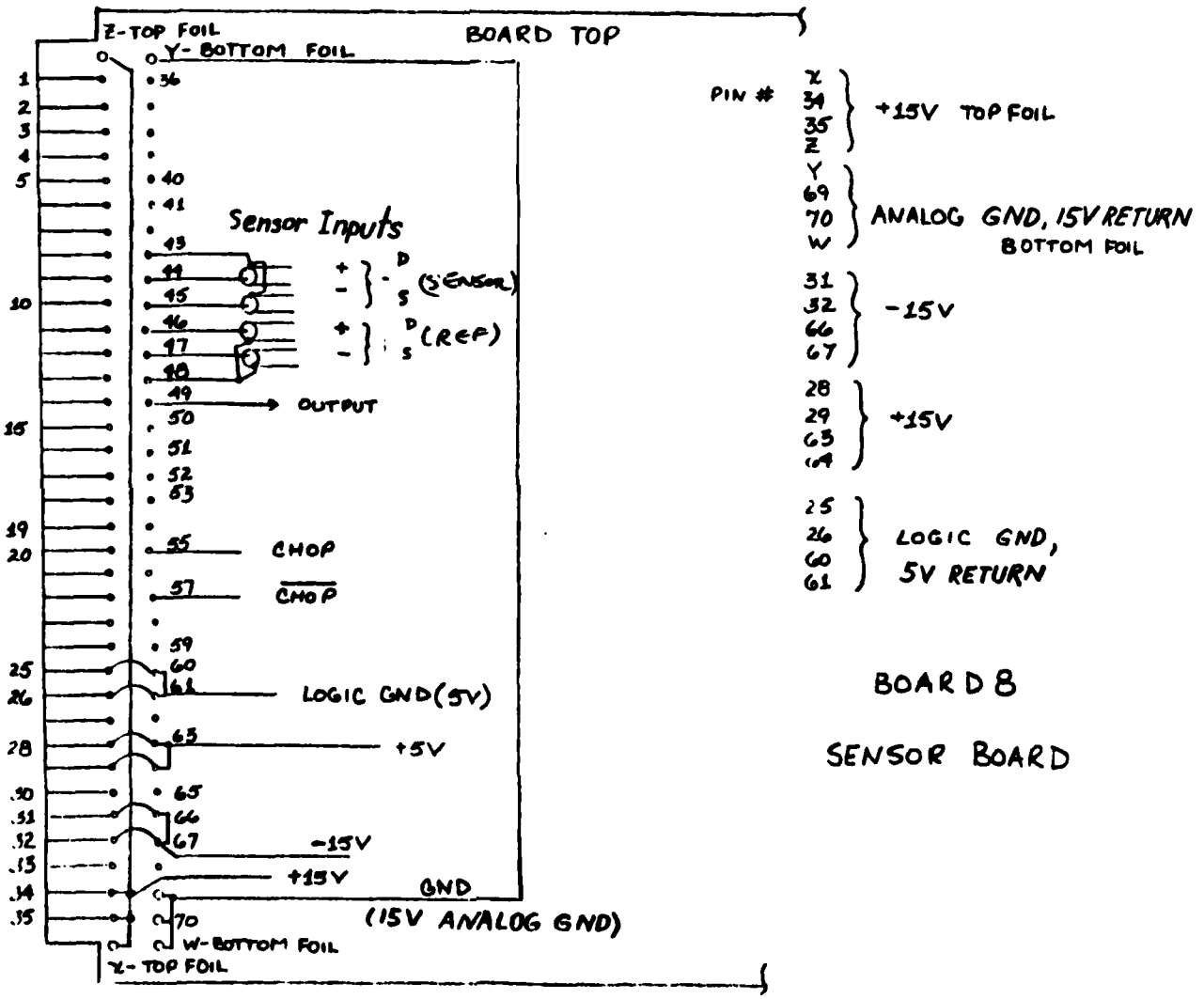

Figure D.9

Back Plane Wiring Diagram for Sensor Interface Board.

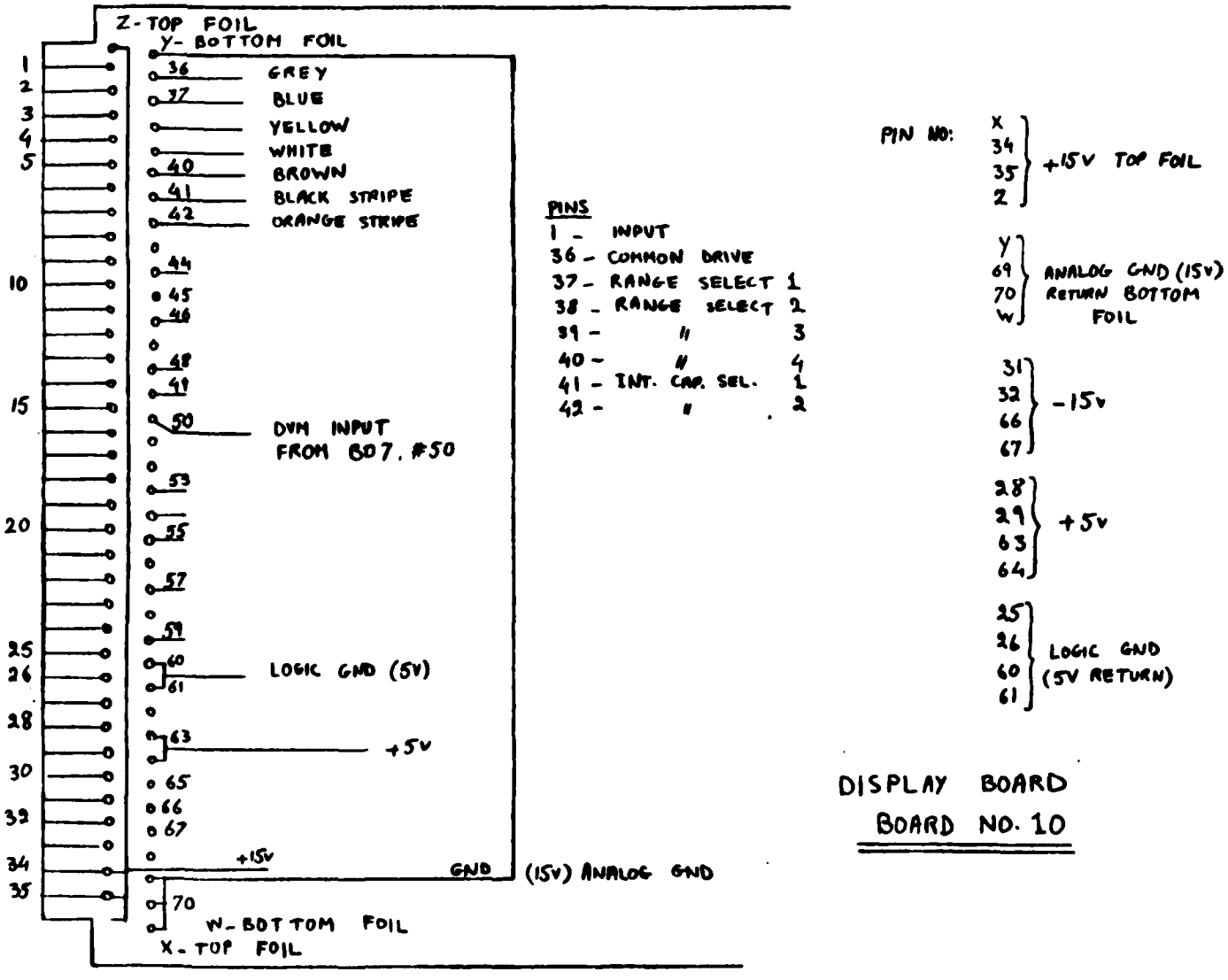

Figure D.10 Back Plane Wiring Diagram for Display Board.

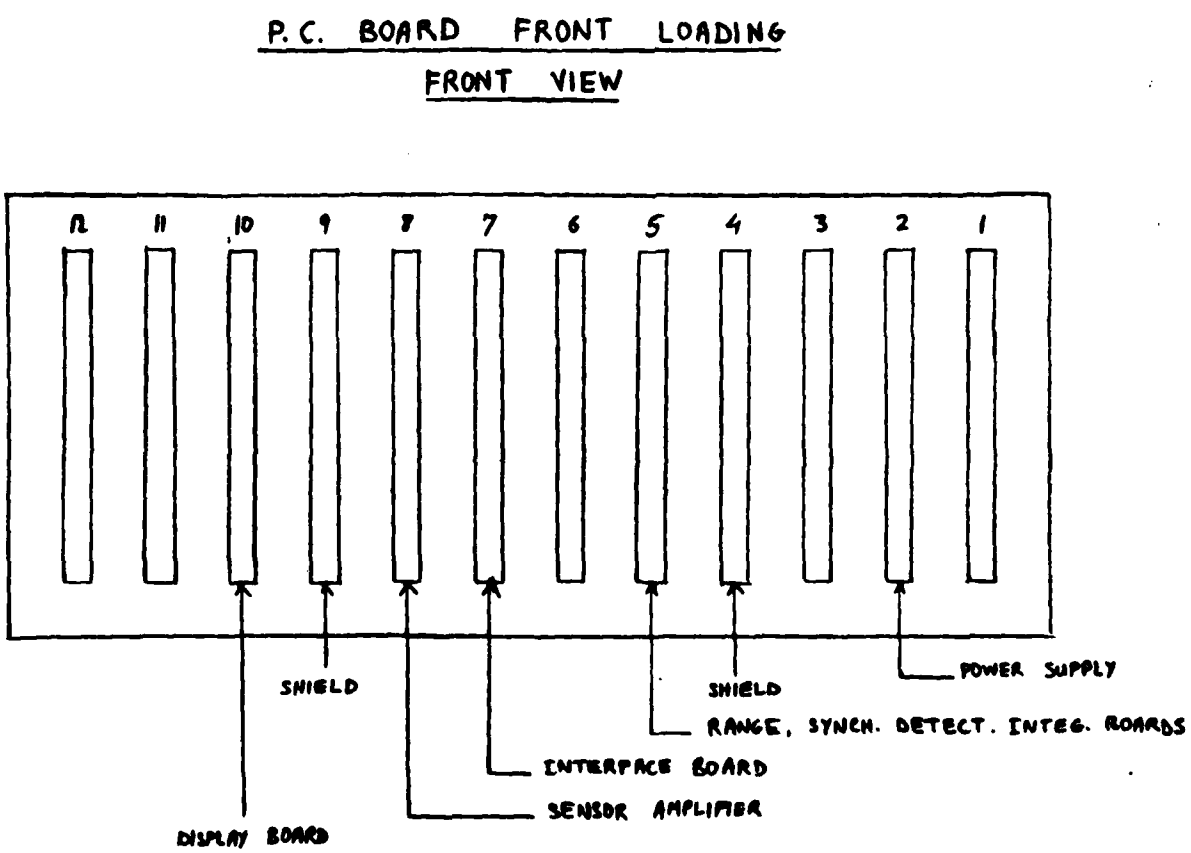

Figure D.11 Front Panel Slot locations.

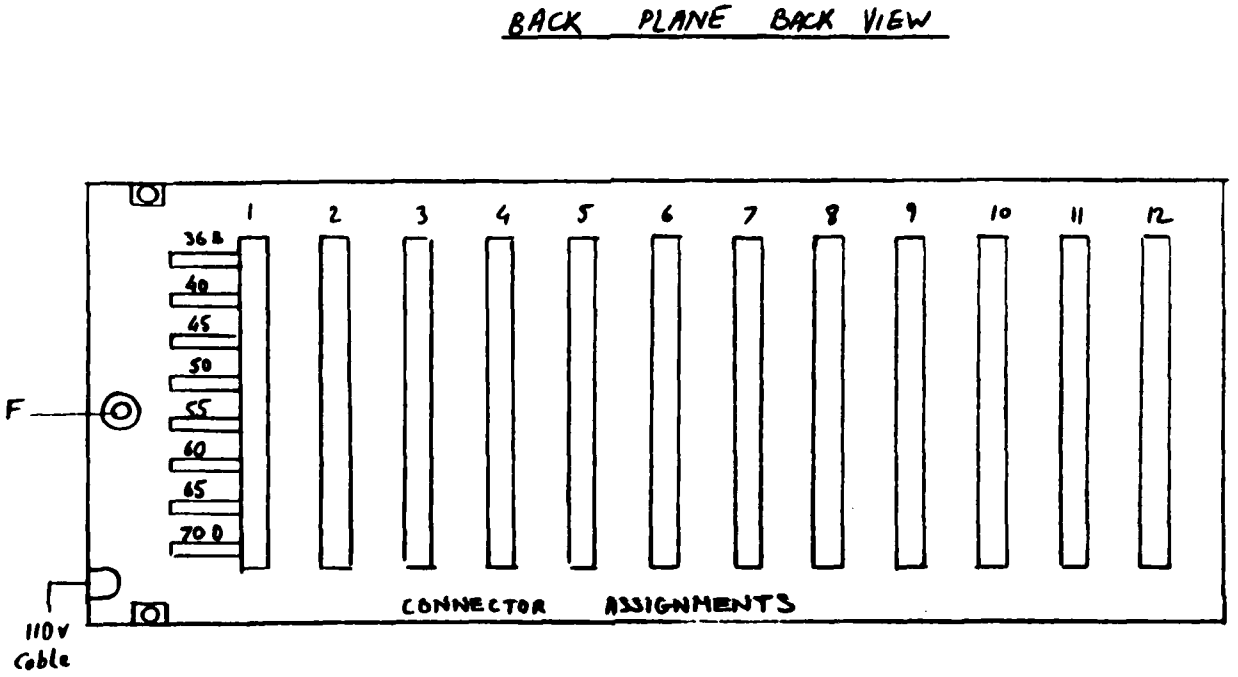

Figure D.12 Back Panel Slot locations.

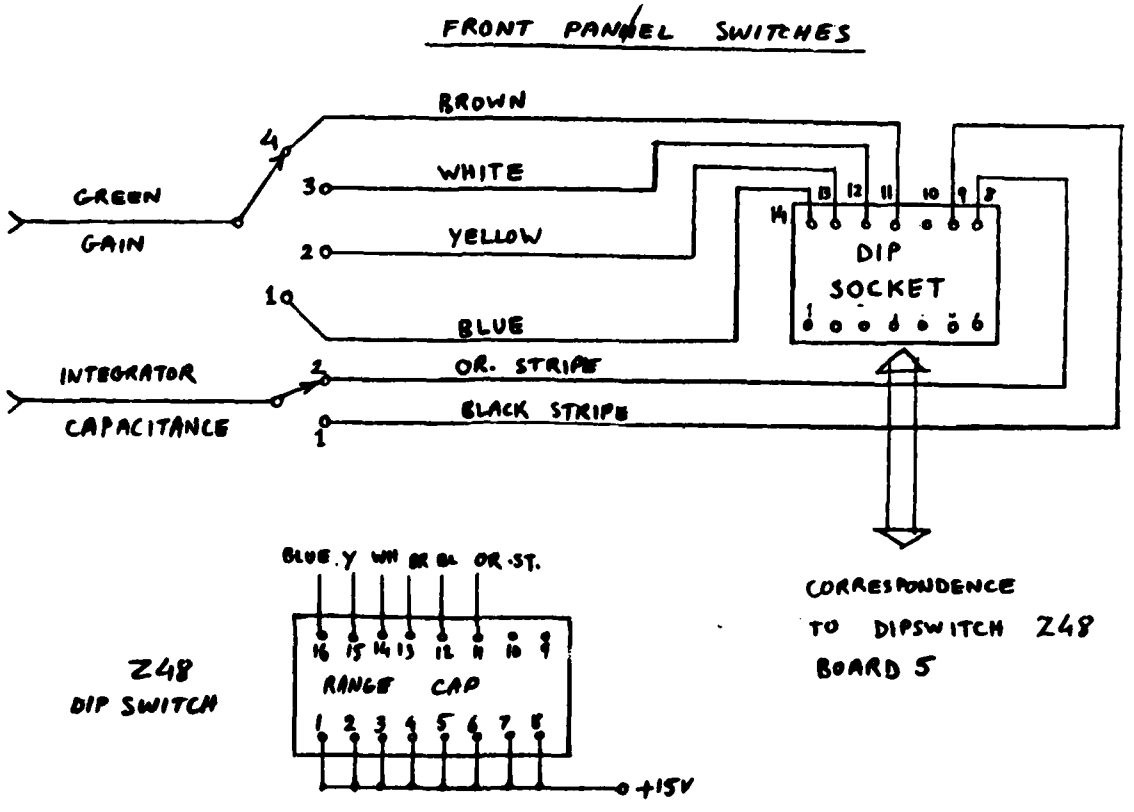

Figure D.13 Switch Color Coding Diagrams.

APPENDIX E - MASTER'S THESIS OF EDMUND J. WALSH

"Floating Gate Field Effect Transistor Operating Point Changes: Causes, Characterization, and Effect of Electric Field Measurment by the Device"

BOSTON UNIVERSITY

College of Engineering

FLOATING GATE FIELD EFFECT TRANSISTOR OPERATING POINT CHANGES: CAUSES, CHARACTERIZATION, AND EFFECT ON ELECTRIC FIELD MEASUREMENT BY THE DEVICE

by

Edmund John Walsh

B.S.E.E., Boston University, 1983

Submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

September 21, 1983

FLOATING GATE FIELD EFFECT TRANSISTOR OPERATING POINT CHANGES: CAUSES, CHARACTERIZATION, AND EFFECT ON ELECTRIC FIELD MEASUREMENT BY THE DEVICE

Edmund John Walsh
Boston University, College of Engineering, 1983

Major Professor: Dr. Mark Horenstein
Assistant Professor of Electrical Engineering

Abstract

A semiconductor device, the Floating Gate Field Effect Transistor (FGFET), was developed at Boston University's High Voltage Laboratory. The device is capable of measuring electric fields without using moving parts, which historically have been necessary for measurement of quasistatic and static electric fields. In actual use, the FGFET operating point has been observed to vary slowly in time. A model for device operation is developed, and an investigation into the causes and characterization of these operating point changes is presented. Finally, using this model, a scheme to limit the effect of these changes when the device is used for field measurement is explored.

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1 INTRODUCTION

Electric field measurement is important in several disciplines like space research and power engineering, where a deficiency has existed in the available techniques for measuring electrostatic and quasistatic fields. Changing fields can be made to produce transient charging currents that can be measured, allowing measurement of the field, but quasistatic fields produce only very small charging currents that are hard to measure, while truly static fields produce none at all. One approach that has been applied successfully to the measurement of quasistatic fields is the use of mechanical chopping to perturb the field. In this scheme, the field sensing electrode is shielded periodically from the field by some type of mechanical motion. As the sensor is alternately exposed and shielded from the field, a measurable transient current is produced, allowing the field magnitude to be determined. This technique is limited because mechanically moving parts are not desirable or feasable in many applications due to space and power requirements.

Another approach to field measurement makes use of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). This solid state, three terminal device responds to voltage changes at its gate terminal by modulating the conductivity between the other two terminals. If the MOSFET is used with

an appropriate detector circuit, these changes in conductivity can be exploited to provide an indication of how the gate voltage has changed. A setup that enables an electric field to modulate the voltage at the gate terminal is shown in Fig 1. In this scheme, a conducting surface is exposed to the field being measured. One segment of the conductor is isolated from the rest of the surface and connected to the gate lead of the MOSFET. Inside the MOSFET, the gate lead is connected to a gate pad, a conducting surface that is isolated from the grounded terminal of the FET by non-conducting paths. In this situation, there is a capacitance between the gate lead and ground. To see how this capacitance gives rise to a voltage at the gate of the MOSFET when an external field is applied, it is helpful to relate the external field to the field between the plates of a capacitor. In Fig 2, a voltage source and a capacitor are used to model the external field, and capacitance from gate pad to ground is also shown. When Cext and Vext are chosen to be consistent with the value of field Eext that actually impinges on the conducting surface, the gate voltage will be determined by the ratio of the external capacitance and the gate to ground capacitance, as in a capacitive voltage divider. In this model, changes in field are represented by changes in the external source. Thus, the gate voltage changes when the external field changes.

The representation of the field sensor shown in Fig 2

is simplified because it does not include the possibility of resistive paths between the plates of the capacitors. Specifically, between the gate pad and ground there are several resistive paths, such as surface leakage, through which the charge on the gate pad could decay. This decay limits the usefulness of the device. For instance, a static field would be measured accurately the instant it was applied, but, as the gate voltage decayed due to the RC decay of the charge at the gate pad, the measurement of the field would become inaccurate. Thus, static field measurements could only be made for times much less than the characteristic time of the RC decay. However, the scheme in Fig 1 is still useful if the fields being measured are not static but change much more quickly than the decay occurs. [5]

In this case, this method of field measurement has many advantages over mechanical chopping. Principally, it has smaller power and space requirements. A technique for measuring fields that has these same advantages, but improves on the deficiencies of a standard MOSFET used to measure electric fields is the subject of this thesis. This technique centers around a semiconductor component, the Floating Gate Field Effect Transistor (FGFET), that is specifically designed for field measurement.

The FGFET is made by modifying commercially available MOSFETs. The bond wire connecting the gate pad of the

transistor to the package header is physically
Obviously, the FGFET is very much like a convention
in structure, except that there are no external co
to the gate pad. In Fig 1, a gate voltage on the M
created by an applied field. This gate voltage
produced a field inside the MOSFET that modi
conduction properties. In the FGFET, the external
intended to be applied directly to the gate p
effectively replaces the conductor segment in Fig 1
gate pad of the FGFET. Because there are no
connections to the gate pad, much of the surface 1
reduced. This improvement gives a much slower rate
of charge induced on the gate pad by the field
fields that vary much more slowly to be measu
enables field measurements of quasistatic fields to
over a longer period of time.

The device has been demonstrated to be ca
measuring electric fields. In actual use, though
been noted that the operating point of the FGFE
stable and tends to drift. The purpose of this the
investigate these changes in operating point, to
their causes, and make a reccomendation as to how t
be eliminated or reduced.

2 OPERATION OF FGFET

The FGFET closely resembles the MOSFET in its structure and operation. Consequently, the significant points of the device geometry can be incorporated into a simple model very much like the models used to describe MOSFETs. Using this simplified geometry, analysis of fields and charge distributions yields a description of device operation.

The major structural components of the FGFET, shown in Fig 3, are the substrate, upon which the device is made, the drain and the source regions diffused into the substrate, a metal gate pad above the substrate regions not covered by the drain or the source, and an insulating oxide layer separating the gate pad from the substrate. If it is assumed conduction occurs strictly in the substrate between the drain and source regions, and if it is also assumed that the events in any cross section are representative of the events in any other cross section, the model need only be two dimensional.

To further simplify the analysis of the device, it is assumed that charge mobility in the substrate is independant of both space and charge density. Particularly, the effect of surface traps at the substrate-oxide interface is not considered. Also, the effects of all interface potentials are ignored. [1]

The substrate may be either lightly doped n- or p-type material with the drain and source heavily doped to be of the opposite type as the substrate. Here, the substrate will be assumed always to be p-type and the source and drain to be n-type. i.e. an "n-channel" device. Dual results for every formula developed using this assumption could be developed for devices with n-type substrate, but all experimental devices used were p-type and no information is lost by considering only p-type devices.

In the device, possible conduction paths between drain and source require charges to move from the drain through the substrate to the source. These paths include a p-n junction from the n-type drain to the p-type substrate and another junction from the p-type substrate to the n-type drain. Such a path is equivalent to two diodes in series, back to back. One diode is always reverse biased and, unless some mechanism changes this situation, no current can flow from the drain to the source. When the drain is positive with respect to the source, electrons would readily move from the substrate to the drain because of the direction of the junction potential at this junction, but electrons would not move into the p-type substrate from the source because the junction potential at the substrate-source junction prohibits such charge movement. Notice that even though the source-substrate junction is such that it would be forward biased if a voltage that is positive from drain to source

were applied across it, it is not possible to forward bias the junction by applying a voltage between the drain pad and the source pad, since this voltage would divide across the substrate-drain and source-substrate junctions. As in the case of back to back diodes, the voltage would be dropped across the reverse biased junction, the substrate-drain junction. The source-substrate junction would not be forward biased above its turn-on point and no current would flow across this junction. Thus, there would be no way to replenish the electrons in the substrate that could flow across the substrate-drain junction, and there would be no steady state flow of electrons from substrate to drain. In this situation, there can of course be no steady state electron current flow from source to drain. By duality, there can be no steady state hole current from drain to source either. i.e. there is no current flow from drain to source. Since the device is symmetrical in this simplified model, even if the polarity of the drain to source voltage is reversed, no current can flow from source to drain either. When a positive electric field is applied to the substrate, free charges move such that electrons from the source and substrate accumulate in the substrate region under the gate pad and holes are expelled from this region by the applied field. The net increase of negative charge in this region will be directly related by Gauss' Law to the magnitude of the field incident upon the substrate. Since

the substrate is lightly doped, resulting in a small amount of free positive charge in the substrate, a relatively weak electric field is required to cause there to be more free negative charge than free positive charge in the region of the substrate affected by the field. The value of field which causes there to be more free negative charges than free positive charges in the region under the gate pad represents a threshold level of field. For field values larger than the threshold, there will be a region under the gate where negative charge carriers predominate. This region is called the inversion layer. (see Fig 4) The presence of the inversion layer allows current to flow from drain to source. Specifically, free negative charges can move from source to drain. The part of the substrate containing the inversion layer has more free negative charges than free positive charges; it is in essence a n-type region. Thus no p-n junction exists between the source and the inversion layer, and the junction potential between source and substrate that prevented the flow of negative charges does not exist in the region of the inversion layer. Negative charges can move into the substrate at the inversion layer, and, as before, these negative charges can move into the drain form the substrate, allowing conduction to occur. The part of the substrate through which conduction takes place is called the channel. In summary, a field that has a magnitude above a certain threshold level, when applied at

the surface of the substrate, can cause an inversion layer to form in the substrate. The inversion layer is n-type and nullifies the source-substrate junction potential, and current can flow from drain to source. The conductivity between drain and source is determined partially by the carrier concentration in the channel. More free charges mean higher conductivity. The carrier concentration is in turn controlled by the magnitude of the applied field. Thus, the conductivity between drain and source can be modulated by an external field. Most significantly, measurement of the external field can be made by observing the current flow from drain to source in the FGFET.

In an unmodified MOSFET, the field modulating the drain to source conductivity results from a voltage applied to the gate by some external source. In the FGFET, there are no connections to the gate pad so no voltage can be applied externally. However, by application of an external field to the FGFET, the conduction properties of the device can be changed. Any external field at the gate pad would necessarily have to satisfy the boundary conditions imposed by the conducting pad. The incident field would terminate on a surface charge in the conductor so that the field in the conductor is zero, satisfying the boundary conditions. The surface charge density on the outer surface of the conductor, by Gauss' Law, would equal the incident electric field density, $\epsilon_0 E_{ext}$. Since the gate pad has a net charge

of zero, the surface charge on the outer surface of the conductor would have an image charge of opposite polarity on the surface of the conductor near the oxide. There would be an electric field originating on this charge. Since the field in the conductor must be zero, the field leaving the gate pad into the oxide layer, by Gauss' Law, must have the same density as the surface charge on the inner surface of the gate pad, which is the same as the charge density on the upper surface, $\epsilon_0 E_{ext}$. The field into the oxide would thus be $\frac{\epsilon_0}{\epsilon_{ox}} E_{ext}$, or $\frac{1}{\epsilon_r} E_{ext}$, where ϵ_r is the relative permittivity of the oxide. This field would also appear at the oxide-substrate interface. Thus, an external field creates a field incident on the substrate like the field in the MOSFET due to the gate voltage, so the external field in the FGFET and the gate voltage applied to the MOSFET produce the same effect - they modulate the conductivity between drain and source. The field applied to the FGFET can be represented by the gate voltage in the MOSFET that would produce the same carrier concentration in the channel region. Relating the externally applied field in the FGFET to a parameter whose effects are well understood in the MOSFET simplifies the derivation of FGFET operating characteristics.

It should be noted that this system as described above is only sensitive to fields that enhance the negative (minority) carriers in the substrate. Fields of opposite polarity, which would make the substrate between drain and

source seem more p-type, have no effect since it is the inversion layer of negative charges that allows conduction across the p-n junction from source to substrate. To allow the device to be sensitive to fields of both polarities, a layer of bound positive charges that act as an "internal bias" can be diffused into the oxide layer above the channel at the time of fabrication. These charges create a field that terminates on negative charges that are drawn into the channel by the field. The inversion layer thus formed allows conduction to take place between drain and source even in the absence of an external field. The conductivity of the channel can still be increased by an external field of appropriate polarity, but it can now also be decreased by a field that diminishes, or depletes, the free minority carriers in the channel that are present because of the bound "biasing" charge in the oxide layer. As with the external field, the fixed charge could also be represented by a voltage on the gate that produces the same carrier concentration in the channel as the fixed charge. To continue the analogy with the MOSFET, a subtle difference will be introduced into the description of this fixed charge, allowing a representation of it that is convenient computationally and easy to determine experimentally. The fixed charge in the oxide layer will be represented by the voltage that would have to be applied to the gate of the unmodified device to cancel the effects of the fixed charge.

This voltage is traditionally called the pinchoff voltage, Vp. (For the p-type substrate device, Vp is negative.) Thus, the bound surface charge can be accounted for by subtracting Vp from the equivalent value of gate voltage that represents an external field. It should be noted that Vp does not represent the voltage applied to the gate that would cancel the electric field associated with the fixed charge. To cancel the effect on current flow in the channel, all of the negative charge carriers drawn into the channel by the fixed charge would not have to be depleted from the channel; the carrier concentration would only have to be reduced below the threshold level. In this way, Vp accounts for both the effects of the surface charge and the existence of a threshold value of field. Experimentally measuring the pinchoff voltage and offsetting the gate voltage by this amount greatly simplifies computations that would of neccesity require consideration of the fixed charge distribution and the threshold phenomenon.

2.1 Mathematical Model of FGFET Operation

The basic operation of the FGFET can be simply stated: Current flows from drain to source due to an applied voltage, Vds. The magnitude of the current for a fixed value of Vds varies directly with the conductivity of the channel.

It has already been described how this conductivity is a function of electric field component normal to the channel, which is represented by an equivalent gate voltage on an unmodified MOSFET. A simplified quantitative description of the current flow in terms of Vds and the equivalent gate voltage can be developed by studying the internal electric fields acting on the free charges in the semiconductor. The net charge density at any point in the substrate is given by the divergence of the electric field. In the two dimmensional model, Ez=0 (Fig 5) so the calculation of the divergance is simplified. Assuming the charge imbalance in the channel is free charge that can contribute to conduction, the current density in the negative y direction (from drain to source) is the product of the electric field in the y direction, the charge density, and the carrier mobility. In reality, some of the total charge in the channel will be fixed charge from the acceptor atoms used to dope the substrate, but the substrate is only lightly doped so the amount of fixed charge is small. Relating Ex and Ey to Vds and Vgs gives a representation of the charge density and current density in the channel in terms of Vds and Vgs which in turn gives drain current in terms of Vds and Vgs. Simplifying assumptions are neccessary to computationally arrive at a usable result. It is assumed that the semiconductor has conduction properties such that the channel region has a thickness, d, that is small compared to

the length of the channel. This is a reasonable assumption. The electric field incident upon the substrate will draw charges toward the surface of the semiconductor. However, as charges begin to accumulate near the surface, a charge gradient exists such that some of the charges drawn to the surface by the field will diffuse back into the semiconductor. Thus, there is a drift current towards the surface and a diffusion current away from the surface. An equilibrium condition will be reached when the drift current equals the diffusion current. It can be shown that at equilibrium the charge density falls off exponentially with distance into the semiconductor and that to a good approximation most of the excess charge drawn towards the surface by the field is within a small distance of the surface, called the Debye length. Though this length depends on many factors, such as substrate doping, it would be typically on the order of one micron or less. [10] In addition, it is assumed that the field is zero at the bottom of the inversion layer. This is also a reasonable assumption because of the high rate of attenuation of the field as it penetrates the semiconductor.

The derivation of the I-V curve of the FGFET to be presented closely follows the derivation in reference [3] of the Id vs. Vds curve of the MOSFET. The major difference between the FGFET and the unmodified MOSFET is what the gate voltage, Vg, actually represents.

Even though the incident field may everywhere be the same above the substrate, a nonuniform charge distribution in the y direction can result in the channel. The voltage in the substrate along the channel thus has a y dependance. Representing the voltage at any point along the channel as V(y) and considering the normal field that draws the charges into the channel to be caused by some equivalent gate voltage, Vg, the normal field in the oxide layer will be related to the voltage difference across the oxide layer by the approximate, quasi one dimensional expression

$$E_o \simeq \left[\frac{V_g - V(y)}{W}\right] \quad 0<y<L \qquad (1)$$

This field expression also represents Ex(0), the field entering the substrate at the semiconductor/oxide interface. To first order, the charge density in the channel will be related via Gauss' Law to this field for any value of y. Since this field, Ex(0), is not uniform in y, there will be an uneven free charge distribution along the channel. Clearly, if the drain voltage, Vd, is larger than Vg and V(y) is a monotonically increasing function for $0<y<L$ then for some values of y, Vg-V(y) will be negative since V(y)=Vd at y=L. At the point Vg-V(y)=0, there will be no normal field at the substrate surface and no excess negative charge in the substrate. For greater values of y, Vg-V(y) will be negative and the normal field components at the substrate surface will be away from the substrate, towards the gate.

There will be an increase in positive charges rather than a buildup of free negative charges in this region of the substrate; the inversion layer will thus stop before it reaches the drain, as depicted in Fig 6. When the inversion layer, which behaves like n-type material, does not extend to the drain, the p-n junction between substrate and drain reforms. Note that negative charges can still flow from the inversion layer to the drain through the depletion region associated with this junction because of the stong electric fields associated with this junction potential.[3] However, the mechanism by which they do so will differ from the case where the inversion layer extends completely across the substrate region from source to drain. Thus, in solving for the drain current as a function of the drain to source voltage, solutions must be developed for two cases. One solution is valid when Vds is less than Vg and no depletion region exists (i.e. the inversion layer extends completely from source to drain), and a different solution, accounting for the formation of the depletion region, is valid when Vds is greater than Vg.

Calculations for both of these cases may be simplified by recalling that both the fixed oxide layer charge and the threshold level of field are incorporated into Vp. Furthermore both the fixed charge and the threshold level can be ignored in calculations by simply offsetting Vg by -Vp after calculations are complete.

2.2 Mathematical Description For Vds<Vg-Vp

Considering first the case where Vds is less than Vg and the channel thus extends the entire length between drain and source, the channel current density is given by the product of the electric field, the free charge concentration, and the carrier mobility:

$$J_y = q \mu_e \Delta n(x) E_y(x) \qquad (2)$$

where q is the electron charge, μ_e is the electron mobility, and $\Delta n(x)$ is the excess negative carrier concentration drawn into the channel by the field.

By integrating the current density over a cross section of the channel in the X-Z plane, the total current from drain to source can be found:

$$I_y = \int_{z=0}^{h} \int_{x=0}^{d} J_y \, dx \, dz \qquad (3)$$

$$I_y = q h \mu_e \int_{x=0}^{d} E_y(x) \Delta n(x) \, dx \qquad (4)$$

where h is the width of the channel in the z direction, perpendicular to the plane of the two dimensional model.

The integral in Eqn (4) is not easy to evaluate because an analytic expression for Ey(x) is not readily obtainable. However, the integral is evaluated over the limits 0 to d, the thickness of the inversion layer, which is assumed to be

very small. It is logical to expect that Ey wou
very little over the range of this integration. I
shown mathematically that Ey is relatively indepen
(i.e. that $\frac{\partial E_y}{\partial x}$ is small) in the channel by co
Faraday's Law

$$\oint_c E \cdot d\ell = 0 \qquad (5)$$

in differential form

$$\frac{\partial E_x}{\partial y} = \frac{\partial E_y}{\partial x} \qquad (Ez = 0)(6$$

Evaluating this relationship at the top of the chan
Ex(0) is known,

$$\frac{\partial E_x}{\partial y} = \frac{\partial}{\partial y}\left[\frac{V_g - V(y)}{W}\right] = \frac{\partial E_y}{\partial x}$$

$$\frac{\partial E_x}{\partial y} = -\frac{\partial}{\partial y}\left[\frac{V(y)}{W}\right] = \frac{\partial E_y}{\partial x}$$

But

$$-\frac{\partial V(y)}{\partial y} = E_y$$

so,

$$\frac{\partial E_x}{\partial y} = \frac{\partial E_y}{\partial x} = \frac{1}{W} E_y$$ (at the top of the

Ex must decrease with x since the field is zero at the bottom of the channel (x = d). It is reasonable to assume that $\frac{\partial E_x}{\partial y}$ also decreases with x since for x > d, Ex = 0 and thus $\frac{\partial E_x}{\partial y} = 0$. [3] Thus, the maximum value of $\frac{\partial E_x}{\partial y}$, and by equality the maximum value of $\frac{\partial E_y}{\partial x}$ occurs at the top of the channel. Considering the differentials to be differences taken over the width of the channel, d, which is a small distance,

$$\frac{\partial E_y}{\partial x} = \frac{1}{W} E_y$$

becomes

$$\frac{\Delta E_y}{E_y} = \frac{\Delta x}{W} = \frac{d}{W} \qquad (10)$$

which gives the maximum change in Ey in the channel as a function of x. For d much smaller than W, the ratio d/W is much less than unity, so the fractional change of Ey over the channel region is very small. Ey can thus be considered to be independant of x in the channel.

Eqn (4) giving the channel current then becomes

$$I_y \simeq q h \mu_e E_y \int_0^d \Delta n(x)\, dx \qquad (11)$$

The integration represents the free charge in the channel for a given value of y. Considering a differential slice of the channel in the y direction, (see Fig 7) this integral can be evaluated using Gauss' Law. Since Ey changes insignificantly over the differential element and Ex=0 at x=d, the total divergence of Ex over the segment $0<x<d$ is Ex(0), which equals the field in the oxide layer, Eo. The charge per unit area in the y direction in the region is then ϵ Ex(0). Remembering Eqn (1):

$$E_o = \left[\frac{V_g - V(y)}{W}\right] = E_x(0) \qquad (1)$$

it follows that

$$q \int_0^d \Delta n(x)\, dx = \epsilon\left[\frac{V_g - V(y)}{W}\right] \qquad (12)$$

where ϵ is the permittivity of the substrate material. Thus, Eqn (11) becomes

$$I_y = h \mu_e \epsilon E_y \left[\frac{V_g - V(y)}{W}\right] \qquad (13)$$

Since Ey is the negative gradient of V(y),

$$I_y = -h \mu_e \frac{\partial V(y)}{\partial y}\left[\frac{V_g - V(y)}{W}\right] \qquad (14)$$

Defining the drain current, Id, as the current that flows from drain to source, the last equation can be rewritten

$$I_d \, dy = \frac{h \mu_e \epsilon}{W} \partial V(y) \left(V_g - V(y) \right) \qquad (15)$$

since Iy must be the negative of the drain current for all values of y. Integrating Eqn (15),

$$I_D \int_0^L dy = \frac{h \mu_e \epsilon}{W} \int_0^{V_{DS}} (V_g - V) \, dV \qquad (16)$$

$$(V_g > V_{ds})$$

yields the familiar formula for drain current in a MOSFET

$$I_d = \frac{h \mu_e \epsilon}{WL} \left[V_g V_{DS} - \frac{V_{DS}^2}{2} \right] \qquad (17)$$

This formula is also valid for the FGFET as long as the gate voltage, Vg, is properly interpreted. In the case of the FGFET, Vg is not some externally applied voltage, and careful consideration must be given to the sources of Vg. It has been stated that the external field as well as the fixed charge in the oxide layer are both modelled by a gate voltage applied to an MOSFET that would produce an analagous effect in the FGFET. It must also be considered that the gate pad is a conductor resistively linked through the oxide

layer to the voltage distribution along the channel. Because of this linking, the voltage at the gate pad will be related to the voltage distribution in the channel. To determine the effect on the gate voltage that this resistive coupling will have, the voltage distribution can be represented as a set of discrete voltage sources linked to the gate pad through resistors (the oxide layer). Ignoring surface conduction, the oxide layer can be modelled as a collection of discrete resistors of equal value. (Fig 8) By linearity it is possible to superimpose the sources that represent the voltage distribution in the channel to show that each source must contribute equally to the gate voltage. Thus, the portion of the gate voltage due to the voltage distribution along the channel is some weighted average of the voltage distribution, V(y). Considering the case where all the voltage sources are the same, it follows simply that Vg will be exactly the average of V(y). When there is no external field and the fixed charge is ignored,

$$V_g = \frac{1}{L}\int_0^L V(y)\,dy \qquad (18)$$

It is this value of Vg, appropriately offset by Vp, that must be used in Eqn (17) to determine the drain current in the FGFET for the case when no external field is applied. The field due to the oxide layer charge can be accounted for

by offsetting the value of gate voltage from Eqn (18) by Vp. Similarly, an externally applied field can be accounted for by offsetting the value of Vg from Eqn (18) by the equivalent gate voltage induced by the external field.

To calculate Vg from the above equation, V(y) must first be determined. Integrating Eqn (15) from 0 to the desired value of y yields:

$$I_D \int_0^Y dy = \frac{h\mu_e\epsilon}{W}\int_0^V (V_g - V)\,dV \quad (19)$$

If Vg is offset by Vp to account for the fixed charge in the oxide layer and the threshold value of field, Eq (19) becomes

$$I_D \int_0^Y dy = \frac{h\mu_e\epsilon}{W}\int_0^{V(y)} (V_g - V_p - V)\,dV \quad (20)$$

or, after performing the integration,

$$I_D Y = \frac{h\mu_e\epsilon}{W}\left[(V_g - V_p)V_{(y)} - \frac{V^2_{(y)}}{2}\right] \quad (21)$$

From Eqn (17),

$$I_D = \frac{h\mu_e\epsilon}{LW}\left[(V_g - V_p)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (22)$$
$$(Vds < Vgs - Vp)$$

Combining Eqn (21) and (22) yields

$$V^2(y) - 2(V_g - V_p)V(y) + \frac{2Y}{L}(V_g - V_p)V_{DS} - \frac{Y}{L}V_{DS}^2 = 0 \quad (23)$$

Solving for V(y)

$$V(y) = (V_g - V_p) + \sqrt{(V_g - V_p)^2 - \frac{2Y}{L}(V_g - V_p)V_{DS} + \frac{Y}{L}V_{DS}^2} \quad (24)$$

where the positive root was chosen to give V(y)=Vds at y=L.

Finally, there are two equations in two unknowns that can be solved for Vg:

$$V_g = \frac{1}{L}\int_0^L V(y)\,dy \quad (18)$$

$$V(y) = (V_g - V_p) + \sqrt{(V_g - V_p)^2 - \frac{2Y}{L}(V_g - V_p)V_{DS} + \frac{Y}{L}V_{DS}^2} \quad (24)$$

Unfortunately, these equations are difficult to solve explicitly for Vg. However, they are easy to solve numerically and are solved in Appendix 1. The numerical solution of Vg can be substituted into Eqn (22) to yield a value of drain current. Thus, for every value of Vds, a

value of Vg can be calculated using the pair of equations, Eqn (18) and Eqn (24), and the drain current as a function of Vds can then be determined using Eqn (17). In this way, the characteristic curve of the device for no external field is determined for values of Vds less than (Vg - Vp).

2.3 Mathematical Description For Vds>Vg-Vp

Eqn (18) and the I-V plot for the FGFET resulting when this equation is solved simultaneously with Eqn (24) are only valid when Vds<Vg-Vp because it was assumed that the voltage in the channel is always smaller than the equivalent value of gate voltage, Vg-Vp. It is quite reasonable to expect that the FGFET will be operated for values of Vds>Vg-Vp, and a mathematical description of device operation must be developed for this range of drain voltages. A straightforward way of deriving those equations is to note the differences between the case where Vds<Vg-Vp and the case where Vds>Vg-Vp. As was indicated in Section 2.0, the major difference that has to be accounted for when Vds>Vg-Vp is the presence of a depletion region at the drain end of the channel. The voltage at one side of the depletion region is the voltage at the end of the inversion layer, Vg-Vp. At the drain end of the depletion region, the voltage is Vds. Though the depletion region is small compared to the rest of the channel, the voltage dropped across it could be

very large. The voltage distribution along the depletion region must therefore be considered in calculating the gate voltage component due to resistive linking of the gate pad to the substrate using Eqn (24).

$$V_g = \frac{1}{L}\int_0^L V(y)\,dy \qquad (24)$$

Since this integral is evaluated along the length of the channel, it can be broken up into two parts, one part representing integration along the inversion layer and the other part representing integration along the depletion region. Thus, Eqn (24) can be written

$$V_g = \frac{1}{L}\left[\int_0^{L-\delta} V(y)\,dy + \int_{L-\delta}^{L} V(y)\,dy\right] \qquad (25)$$

The two integrals in Eqn (25) can be considered to be the sum of the average voltage along the inversion layer weighted by the fraction of the channel occupied by the inversion layer plus the average voltage along the depletion region weighted by the fraction of the channel occupied by the depletion region. This interpretation suggests that the actual channel length is not important. Rather, it is only the relative proportions of the channel occupied by the inversion layer and the depletion region that is of significance. To simplify calculations, the channel length, L, can be normalized to unity, and the normalized length of the depletion region, δ_n, can be interpreted as the fraction of the channel occupied by the depletion region. In

normalized form, Eqn (25) becomes

$$V_g = \int_0^{1-\delta_n} V(y)\,dy + \int_{1-\delta_n}^{1} V(y)\,dy \qquad (26)$$

The depletion region, because it is like the depletion region associated with any p-n junction, is short in comparison to the channel length, which is on the order of tens of microns for a typical device compared to tenths of a micrometer for a typical depletion region. [8] The realization that the depletion region is short relative to the inversion layer and to the overall channel length allows a simplification of Eqn (26). The fraction of the channel occupied by the depletion region, δ_n, must be small - much less than 1. The first integral of Eqn (26) is evaluated from 0 to $1-\delta_n$. Since δ_n is much smaller than 1, $1-\delta_n$ is very close to 1, and the equation is not changed appreciably by considering the upper limit of the first integral to be 1.

$$V_g \simeq \int_0^{1} V(y)\,dy + \int_{1-\delta_n}^{1} V(y)\,dy \qquad (27)$$

The same simplification can not be made in the second integral since it would eliminate that term and V(y) may be large in the depletion region. However, the second integral can still be simplified. The second term of Eqn (27) represents the average voltage along the depletion region weighted by the fraction of the channel occupied by the

depletion region, δ_n. The voltage at one end of the depletion region, the end at the inversion layer, is Vg-Vp. The other end of the depletion region is at a voltage Vds. Since the depletion region is so short, minimal error is introduced by considering the voltage in the depletion region to change linearly between these two endpoints. Thus the average voltage in the depletion region is

$$\frac{1}{2}\left((V_g - V_p) + V_{DS}\right)$$

and the second integral of Eqn (27) could be replaced by

$$\frac{\delta_n}{2}\left((V_g - V_p) + V_{DS}\right)$$

which represents the average voltage in the depletion region weighted by the fraction of the channel occupied by the depletion region. Eqn (27) thus becomes

$$V_g \simeq \int_0^1 V(y)\,dy + \frac{\delta}{2}\left((V_g - V_p) + V_{DS}\right) \quad (28)$$

What remains is to determine the voltage distribution, V(y), that should be substituted into the first integral. The integration represents the average voltage along the inversion layer, which extends from the source to very nearly to the drain. The voltage at the end of the inversion layer is of course Vg-Vp. An equation to describe the voltage distribution along the inversion layer was developed in the consideration of the case when Vds<Vg-Vp:

$$V(y) = (V_g - V_p) + \sqrt{(V_g - V_p)^2 - \frac{2y}{L}(V_g - V_p)V_{DS} + \frac{y}{L}V_{DS}^2} \quad (24)$$

Eqn (24) gave the voltage distribution along an inversion layer that extended to the drain and ended where the voltage was Vds. In the present case, though the inversion layer to be described by the equation extends nearly to the drain, the voltage at the end of the inversion layer is Vg-Vp rather than Vds. Eqn (24) must be modified by replacing Vds by Vg-Vp.

$$V(y) = (V_g - V_p) + \sqrt{(V_g - V_p)^2 - \frac{2y}{L}(V_g - V_p)(V_g - V_p) + \frac{y}{L}(V_g - V_p)^2} \quad (29)$$

After simplification this equation becomes

$$V(y) = (V_g - V_p)\left(1 - \sqrt{1 - y/L}\right) \qquad \begin{matrix} 0 < y < 1 - \delta_n \\ V_{DS} > V_g - V_p \end{matrix} \quad (30)$$

This value can be substituted into Eqn (28) to yield an expression for gate voltage.

$$V_g = \int_0^1 (V_g - V_p)\left(1 - \sqrt{1 - y/L}\right) dy + \frac{\delta}{2}\left((V_g - V_p) + V_{DS}\right) \quad (31)$$

Solution of this equation for one unknown, Vg, is straightforward. The result is

$$V_g = \frac{-2V_p + 3\delta_n(V_{DS} - V_p)}{4 - 3\delta_n} \quad (32)$$

This equation for Vg is neccessary to calculate an I-V plot for the FGFET. However, an expression for δ_n must be determined before this equation can be useful. Examination of the I-V plot of an unmodified MOSFET (Fig 9) indicates how δ_n can be determined using experimental measurements on an unmodified MOSFET.

The familiar I-V plot of an unmodified MOSFET is shown in Fig 9. The curve Vds=Vg-Vp is indicated on the plot. The inversion layer for values of Vds less than Vg-Vp acts somewhat like a constant resistance so the drain current increases as the drain voltage increases. The decreasing slope of the I-V curve as Vds approaches Vgs-Vp is due to the fact that the shape of the inversion layer is changing. The inversion layer gets thin near the drain for values of Vds near Vg-Vp. This decrease in size has the effect of increasing the effective resistance(decreasing slope) as Vds increases. At Vds=Vgs-Vp, the inversion layer disapppears at the drain end of the channel. This occurance is commonly called pinchoff. At pinchoff, the depletion region begins to form. The path for electrons from source to drain thus includes the inversion layer and the depletion region associated with the p-n junction between substrate and drain. The electrons are rapidly accelerated through the depleton region because of the p-n junction potential across the region. Current flow is not limited by the depletion region. Rather, current is limited by the amount of charge that can flow through the inversion layer to the depletion region. After pinchoff, the inversion layer has a constant voltage, (Vg-Vp), across it, so the current flow is nearly constant after pinchoff, as shown in Fig 9. The slight increase in current flow as Vds increases past pinchoff can not be due to a larger voltage across the inversion layer.

Rather, the effective resistance of the inversion layer decreases. The decrease in resistance is a result of the inversion layer getting shorter as Vds is increased. The increased voltage across the depletion region causes a slight increase in its physical dimensions, requiring that the inversion layer be slightly shorter, and allowing the drain current to increase slightly. A measurable device parameter can thus be related to the length of the depletion region, which allows determination of δ , the depletion region length, by experimentally observing the rate of change of current, $\frac{\partial I_D}{\partial V_{DS}}$, in an unmodified MOSFET for values of Vds greater than Vgs-Vp.

This rate of change, $\frac{\partial I_D}{\partial V_{DS}}$, is the reciprocal of the dynamic resistance at the point the derivative is evaluated. Based on experimental observation, it is reasonable to consider this value to be nearly constant over the range of drain to source voltages of interest. This dynamic resistance is often given the symbol r_o . Thus,

$$r_D = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} \qquad (33)$$

To make use of this expression, an equation for Id for Vds>Vg-Vp can be determined from Eqn (22). The current flow for the range of Vds values greater than Vg-Vp is determined by the shape of the inversion layer, principally its length. This length is L- δ . Moreover, the voltage across the inversion layer is Vgs-Vp. Using Eqn (22),

$$I_D = \frac{h \mu_e \epsilon}{WL} \left[(V_g - V_p) V_{DS} - \frac{V_{DS}^2}{2} \right] \qquad (22)$$

to represent the current flow through the inversion described, the length L in Eqn (22) would be replace appropriate length, $L-\delta$. Moreover, the voltage ac inversion layer in Eqn (22), Vds, would be replace appropriate voltage, Vgs-Vp. Thus the current f Vds>Vgs-Vp is given by

$$I_D = \frac{h\mu_e\epsilon}{W(L-\delta)}\left(\frac{(V_{gs}-V_p)^2}{2}\right) \qquad ($$

Using Eqn (23) in the inverse of Eqn (33) yields

$$\frac{1}{r_o} = \frac{\partial I_D}{\partial V_{DS}} = \frac{h\mu_e\epsilon}{W}\left(\frac{(V_{gs}-V_p)^2}{2}\right)\frac{\partial}{\partial V_{DS}}\left[(L-\delta\right.$$

Since δ is the only variable that is a function of equation as written still apllies to an unmodified this equation can be rewritten

$$\frac{1}{r_o} = \frac{h\mu_e\epsilon}{W}\left(\frac{(V_{gs}-V_p)^2}{2}\right)(L-\delta)^{-2}\frac{\partial\delta}{\partial V_{DS}}$$

Recognizing that the expression for Id is still cont Eqn (36), a simpler expression results:

$$\frac{1}{r_o} = I_D\left(\frac{1}{L-\delta}\right)\frac{\partial\delta}{\partial V_{DS}} \qquad (3$$

Rearranging the terms

$$\frac{\partial\delta}{\partial V_{DS}} + \frac{1}{r_o I_D}\delta = \frac{L}{r_o I_D} \qquad (3$$

Though δ depends on Vgs as well as Vds, this equation can be limited in application to places where Vgs is constant. Thus Eqn (38) becomes

$$\frac{d\delta}{dV_{DS}} + \frac{1}{r_o I_D}\delta = \frac{L}{r_o I_D} \qquad (39)$$

Eqn (39) is a first order differential equation whose solution can be determined by applying the boundary condition that $\delta = 0$ for Vds=Vgs-Vp. Thus,

$$\delta = L\left(1 - \exp\left[-\left(\frac{V_{DS} - (V_{gs} - V_p)}{r_o I_D}\right)\right]\right) \qquad (40)$$

To summarize the derivation so far, there are three equations in the variables δ, Id, and Vgs. These quantities are all directly or indirectly interrelated.

$$V_g = \frac{-2V_p + 3\delta_n(V_{DS} - V_p)}{4 - 3\delta_n} \qquad (32)$$

$$I_D = \frac{h\mu_e\epsilon}{W(L-\delta)}\left(\frac{(V_{gs}-V_p)^2}{2}\right) \qquad (34)$$

$$\delta = L\left(1 - \exp\left[-\left(\frac{V_{DS} - (V_{gs} - V_p)}{r_o I_D}\right]\right)\right) \qquad (40)$$

Normalizing Eqns (34) and (40) to the channel length gives a more convenient representation.

$$I_D = \frac{h\mu_e\epsilon}{W(1-\delta_n)}\left(\frac{(V_{gs}-V_p)^2}{2}\right) \qquad (34)$$

$$\delta_n = 1 - \exp\left[1 - \left(\frac{V_{DS} - (V_{gs} - V_p)}{r_o I_D}\right]\right] \qquad (42)$$

Eqn (32) applies specifically to a FGFET. Eqns (41) and

(42) were determined for a MOSFET, but, again, they also apply to the FGFET if the voltage Vg is replaced by the gate voltage given in Eqn (32). The resulting set of equations can be solved numerically to yield the I-V plot for the FGFET for Vds>Vg-Vp.

3 DETERMINATION OF IV CHARACTERISTICS

Equations (18), (22) and (24) describe the operation of the FGFET when Vds is less than Vg-Vp, and Eqns (32), (41) and (42) describe device operation for larger values of Vds. These groups are sets of independant equations that can be solved for any or all of the variables. Finding such solutions would allow determination of the I-V operating characteristics of the device. However, explicit solutions to the equations are complicated. Fortunately, solutions are readily obtained numerically using a digital computer. The governing equations of the FGFET have been incorporated into a PASCAL program to predict current and voltage operating points of the FGFET. The details of the algorithm to solve these equations simultaneously are presented in Appendix 1. A sample output of this program is shown in Fig 10, and these theoretical predictions are compared to experimental data in Section 5, where the imperfections of this mathematical model are examined.

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4 FGFET RESPONSE TO INCIDENT FIELD

Since the FGFET is intended to be used as a field sensor, it is relevant to investigate how a field incident on the gate pad will affect the I-V characteristics of the device. The procedure for calculating the unexcited I-V curve, detailed in Appendix 1, can be modified to produce the desired results, since the same equations apply to the operation of the device when a field is applied.

The equivalence of an electric field normal to the FGFET substrate and a voltage applied to the gate pad has been justified in the derivation of the device I-V curve. This relationship may again be used to simplify the determination of the effects of an external field. The gate to substrate potential is calculable by applying the field equation

$$V = -\int_{x=w}^{0} E \cdot d\ell \qquad (43)$$

to a path connecting the gate pad and substrate. When only the component of gate voltage caused by the external field is considered, the substrate surface may be assigned zero potential. In this case, Eqn (43) reduces to

$$V_g = E \cdot W \qquad (44)$$

where E is the field in the oxide layer and W is the width of the oxide layer. In Section 2, it was shown that the oxide layer field is related to an externally applied field

striking the gate pad by the relative permittivity of the oxide layer:

$$E = \frac{1}{\epsilon_r} E_{ext} \qquad (45)$$

Using Eqns (44) and (45), an external field is easily related to the gate voltage it would produce,

$$V_g = \frac{1}{\epsilon_r} E_{ext} \cdot W \qquad (46)$$

Immediately after a field is applied, its effects can be represented by offsetting the gate voltage by the value given in Eqn (46). Recall, though, that offsets in the gate voltage have been lumped into the parameter Vp. Thus, fields incident on the gate pad produce the same effect on the I-V curve as changes in Vp. The PASCAL program used to calculate the curve can be easily adjusted for such changes.

The amount by which Vg must be changed depends on the width, W, and the relative permitivity of the oxide layer. The width depends on the specific process by which the MOSFET is made, but for commercially available devices W is on the order of 1000A. For silicon dioxide, ϵ_r is about 4. [1] A field of 100kV/m incident on the gate would thus be equivalent to an applied offset in Vg on the order of 2.5mV. The calculated I-V curve of the FGFET is shown in Fig 11 with the applied field as a parameter. Notice that the changes in operating point are actually very small for practical fields since the applied fields shown in Fig 11

are orders of magnitude larger than are to be measured or could even exist in air. Nevertheless, it is these small changes in operating point with applied field that make the FGFET useful as a field measuring device.

5 DEVIATIONS FROM MATHEMATICAL MODEL

The model derived to describe FGFET operation is based on a simplified description of the device. There are two major effects not included in the model that signifiacantly affect device performance. An acceptable model must include these effects.

The prediction of the static I-V curve of the FGFET shown in Fig 10, based on a computer solution of describing equations of an idealized device, differs significantly from the actual curves based on experimental measurements. Experimental data is presented in Fig 12 for comparison with the theoretical plot of Fig 10. In the development of the equations to predict the I-V curves, it was assumed that the voltage at the gate pad was a result of resistive linking through the oxide layer of the gate pad to the voltage distribution in the substrate. The voltage distribution in the channel does affect the voltage at the gate, but is not the only factor determining the equilibrium gate voltage.

The drain and source, like the channel in the substrate, are at potentials different from the gate pad potential. The voltages at the drain and source, since both are linked to the gate pad through surface conduction paths, also add components to the voltage at the gate. The gate pad can be thought of as the midpoint of a resistive voltage divider between drain and source in addition to being linked through the oxide to the channel voltage distribution. To

first order, the voltage at the gate due to the resistive linking to drain and source can be considered to be a constant fraction of the drain to source voltage. In the calculation of the I-V curve, this linking effect can be included by offsetting the gate voltage by a certain fraction of the drain to source voltage. The PASCAL program used to calculate the I-V curve in Fig 10 has been modified to consider the resistive linking between drain, source and gate. The output of this program is shown in Fig 13. The curve is computed for a range of values of the fraction of drain to source voltage linked to the gate. The actual value of this fraction is hard to determine, except by comparison with experimental data, since the resistance of the surface conduction paths depends on device geometry as well as external factors, such as humidity and ion concentration in the environment, that would change surface conductivity. It appears from comparison of Fig 12 and Fig 13 that the actual value of the resistive coupling coeficient is near 0.2 or 0.3 because the theoretical curves with this amount of coupling have the same shape as the experimental curves.

Secondly, the equation to derive the I-V curves for the device implicitly assumed equilibrium of charges and fields since equilibrium equations were used. The charge distribution in the channel will induce a voltage on the gate as predicted. However, the oxide layer that links the substrate to the gate pad has a very high resistance and the

charge rate of flow through this layer will be proportionately slow. It will take time for the device to reach the equilibrium dictated by the resistive linking to the voltage distribution in the channel and the resistive linking to drain and source because it takes time for the charge needed at the gate to establish the equilibrium to reach the gate. Thus, there is a time varying component of the gate voltage that must be considered in the description of the device operation.

When a voltage is applied from drain to source with the gate pad initially having no net charge on it, the charge on the gate pad will, for an instant after the drain to source voltage is applied, remain unchanged since charge moves to the gate very slowly through the resistive paths from substrate, drain or source. The charges on the gate pad will redistribute within the conductor in response to the field associated with the drain to sorce voltage. A schematic view of the charge distribution and field pattern is shown in Fig 14. Notice there is an electric field that originates on the drain pad and terminates on the gate pad. Such a field is analagous to the field between the plates of a capacitance connected between drain and gate. Similarly, the field between gate and source can be represented by a lumped capacitance as shown in Fig 15. The gate pad is like the middle node of a capacitive voltage divider. Immediately after a voltage is applied from drain to source, the gate

voltage will be determined by the ratio of the lumped capacitances - as in a capacitive voltage divider. Eventually, though, charges will difffuse across the surface and through the oxide layer and the gate voltage will approach the equilibrium value determined by the resistive linking. The rate at which the gate voltage approaches its equilibrium value is determined by the rate at which charges move through the oxide layer and through surface conduction paths. The analogy can be made to an RC circuit like the one in Fig 16.

To the surprise of every electrical engineering student, circuit theory analysis of the circuit in Fig 16 provides useful information about how the FGFET responds to changes in Vds. For example, when Vds is first applied, the gate voltage will be determined by the capacitive voltage divider C1 and C2. The gate voltage, though, must eventually satisfy the steady state value determined by the resistive divider R1 and R2. Thus, the gate voltage will change instantaneously when Vds changes, and will then exhibit a transient change as it approaches steady state. Analysis predicts that the transient will be a first order exponential. As a result of this transient, the I-V operating point of the device will have a time dependence, since the operating point depends directly on the gate voltage, which contains transient components. Experimentally, the transients associated with changes in

Vds have been measured and are exponential with a time constant on the order of one to four hours. Experimental data of a representative measurement is presented in Fig 17. The specific technique used to gather this data is described in Appendix 4. A theoretical understanding of the nature and origin of the time dependant components of FGFET operating point provides an important step in understanding and eliminating them.

Fig 16 predicts two types of changes in the gate voltage - instantaneous and transient changes - are possible. This model can be readily extended to predict changes in the device operating point on an incremental level, and to show that changes in the operating point are characterized by the same types of changes that characterize changes in gate voltage. To relate the model for Vg vs. Vds to a model that predicts Id vs. Vds, Id must be related to Vg. In analysis of unmodified MOSFETs, the ratio $\Delta Id/\Delta Vg$ is termed the transconductance when the ratio is evaluated near the actual device operating point. Id is not linearly related to Vg, but for Vg nearly constant, $\Delta Id/\Delta Vg$ can be considered to be a constant. The ratio of the change in drain current to the change in gate voltage is usually given the symbol "gm," which will be used here. The steady state operating point is different for every value of Vds in the FGFET. The analysis presented in previous sections shows that the gate voltage is not linearly related to Vds. Thus

over the entire range of Vds, the ratio of the resistors in the model of Fig 16 depends on the value of Vds at which the model is to be applied. However, in considering small changes in parameters with Vds nearly constant, the ratio Vg/Vds at steady state will be nearly constant, and the resistors incrementally can be considered to be constant valued. The capacitance is largely a function of device geometry and so the capacitors in the model are independant of operating point. The resulting model, that is most accurate when used to analyze variations around a given operating point, is shown in Fig 18. This model can predict qualitatively how the FGFET will respond to various stimulus. For qualitative predictions, it is not necessary to determine the values of each of the components. It is worth noting, though, that unlike the capacitors which can be associated with a specific capacitance, the resistors do not represent fixed physical resistors, but represent the conglomeration of all factors that affect the steady state operating point. Recalling the derivation of the steady state I-V curve for the FGFET, the factors that affect the steady state gate voltage are the resistive linking of the gate to drain, source, and the voltage distribution in the channel, V(y). Since V(y) depends on Vds, but not linearly, the resistor values in the model will be different for every value of Vds and must be such that the resistive divider gives

$$V_g = \frac{R_2}{R_1 + R_2} V_{DS}$$

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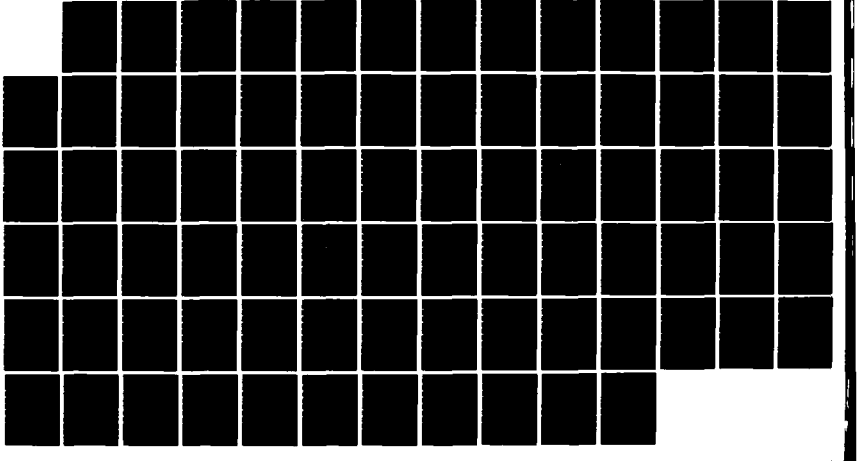
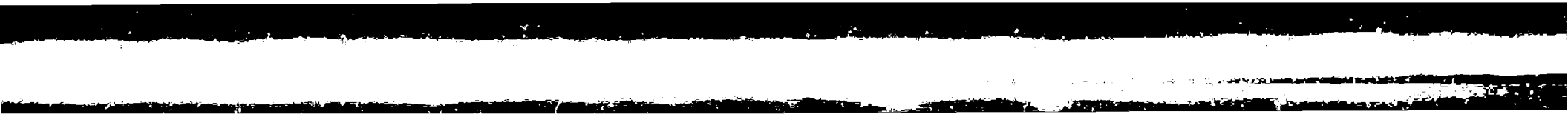
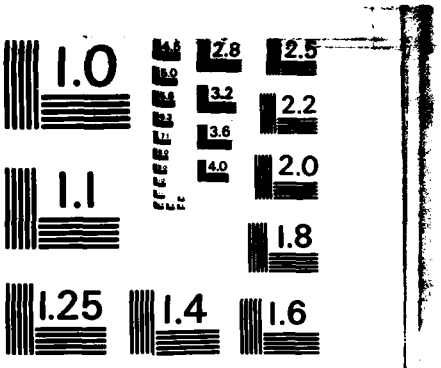






near the value of Vds in question. The model must also predict the correct time constant for the circuit, so

$$\tau = (R_1 \| R_2) \cdot (C_1 \| C_2)$$

must equal the actual time constant. The ratio of resistors indicates the steady state gate voltage and the value of the parallel combination indicates the time constant of the decay.

5.1 Changes in FGFET Operating Point

Since the FGFET is intended to be used as a field measuring device, it is important to be able to predict how external factors that may be prevalent when the device is used affect the operating point. Once these effects are understood and characterized, steps can be taken to prevent these operating point changes from affecting measurements made by the FGFET while it is used as a field sensor. The model of Fig 17 gives insight into how various factors affect the FGFET operating point. Since changes in the device operating point due to external factors could be mistaken for changes in the device operating point due to an input field, it is important to consider as many factors as possible that affect the operating point.

Changes in Vds have already been discussed. They produce an instantaneous change followed by an exponential transient. This behavior is typical of any factor that

instantaneously changes the operating point - even the application of an external field to be measured. For example, changes in temperature produce this type of behavior because the carrier concentration in the substrate changes with temperature which in turn changes the channel conductivity. For a fixed value of Vds, Id must then also change with temperature. This change is represented in the model of Fig 18 by allowing gm to change instantaneously with temperature (n.b. the operating point will change as quickly or as slowly as the temperature). Recall from the solution of the steady state equations of the FGFET that the steady state gate voltage is dependant on the carrier concentration in the substrate because V(y) depends on the carrier concentration. Temperature, since it changes the carrier concentration must also affect the steady state operating point. This dependance would be shown in the model by changing the ratio of the resistor values - but not the value of the parallel combination of R and C since changing that value would change the time constant. Thus, an instantaneous change in temperature gives rise to an instantaneous and a time dependant change in the operating point. Light striking the semiconductor substrate would produce exactly the same effect since light would change the substrate carrier concentration also. In the FGFET, the gate pad and the oxide layer cover most of the substrate, so light is not a major factor. However, depending on the

fabrication of the device, light could affect the operating point. Application of field signals also produces an instantaneous and a transient change in operating point. The instantaneous change due to an input field was discussed previously, and can be represented in the incremental model by a voltage source capacitively linked to the gate. The incremental model is shown modified in Fig 19. Analysis shows that initially the field will change the gate voltage and thus the FGFET operating point, but the steady state value of gate voltage, as determined by the resistors, will not change. Even though a field is continuously applied, the operating point will approach the same steady state as if there was no applied field. Moreover, it will return to this state with an exponential transient. For Cext much smaller than C1 or C2, as would normally be the case, the transient will be nearly the same frequency as the characteristic decay of the FGFET. In the case of transients associated with field measurement, the decay components are unwanted because they represent a reduction in the desired output signal.

The above cases indicate that a transient response may be generated when the operating point of the circuit changes instantaneously. It is possible that the steady state operating point may change, thus creating a transient decay towards the new steady state value, without an associated instantaneous change. Any factor that changes the surface

ion concentration - humidity, for example - would cause a change in the surface conductivity. This change would affect both the steady state gate voltage and the time constant of the decay towards this steady state. Changes in surface conductivity would be represented in the model by a change in the ratio of the resistors and by a change in the value of the parallel combination of the resistors. Notice, though, that changes in surface conductivity do not produce an instantaneous change in the operating point since the capacitive components of the model are not affected in any way. Changes in surface conductivity could explain why the characteristic time constant has been experimentally found to vary.

All of the factors that affect the operating point - either by instantaneously changing it or by engendering a transient component in it - will reduce the usefulness of any circuit utilizing the FGFET to measure electric fields since these effects would produce false output signals. At present, work at Boston University's High Voltage Laboratory, where the FGFET is being developed for use in an electric field probe, has centered around minimizing offending external factor variations. Significant stabilization of FGFET operating point has been demonstrated at BUHVL by maintaining a constant temperature environment and by using the device only after the transient associated with initial application of Vds has died away. A refinement

to this approach will be investigated here. The method will be based on recognizing that changes in operating point take two forms, instaneous and exponential. The method to be developed here will specifically address the issue of reducing the effects of transient changes in the FGFET operating point on any circuit that utilizes the FGFET for field measurement. The procedure will not be effective against instantaneous changes in device operating point. The major benefit that should be derived from suppressing transient changes in operating point is that the output signal will more accurately represent only the effect of an input signal field. The effects of initial application of Vds, the unwanted transient associated with the application of a field, and the transients associated with any other changes in device operating point will all be reduced.

The transients that this method will be designed to eliminate are the ones with exponential time constants that are close to the characteristic time constant of the device. Experimental data presented in Fig 17 indicates that this time constant is on the order of one hour to several hours. This variation is a very slow one. Most notably, it is slower than the expected changes in electric fields that are to be measured by the device. It may therefore be possible to identify and separate the transient components from the signal components in the output of a circuit using the FGFET based on the frequency properties of the output signal.

6 FGFET AS A FIELD SENSOR

The FGFET was developed for the purpose of measuring electric fields that vary quickly and slowly in time. An electric field incident on the gate will induce or deplete charge carriers in the channel, thus changing the conductivity of the channel. To sense a field, the minimum requirement is that this change in conductivity be manifested as a change in some measurable circuit parameter.

A simple circuit that meets this criterion would have only a fixed voltage source and a resistor in series with the FGFET as shown in Fig 20. The external field would change the I-V characteristic of the FGFET and the current flow in the circuit would change. The change in current flow would cause a measurable change in voltage across the resistor. A problem with this scheme is that for the field signal to be measurable, the drain voltage must change appreciably, and Vds, in this circuit, will change significantly in response to the input field. Such a change represents a change in the device operating point and a new steady state value of gate voltage. Recall that it takes a long time, on the order of hours, for the device to reach steady state. The transient as the FGFET approached steady state would appear as a drift in the output as a function of time. This time dependance of the output is undesirable not only because the output will change for a constant input,

but also because until the output reaches steady state, it will depend on previous values of the gate voltage. Such a situation makes this circuit undesirable for application as a field measuring device. A better circuit for field measuring applications would drastically restrict any changes in device operating point when an input signal is applied.

An ideal model of a circuit designed to restrict the operating point of the FGFET is shown in Fig 21. The actual schematic to implement the circuit is shown in Fig 22. In the ideal model, the drain to source voltage is fixed by the voltage source that keeps the drain at a constant voltage above the source. The signal field modulates the current flow through the device. Since a constant current always flows through the current source, any changes in current through the FGFET must flow through the resistor Ro. The current flow through the resistor changes the voltage drop across the resistor which in turn changes the source voltage. This makes a measurable change directly related to the magnitude of the input field. Of course the drain to source voltage does not change so there can be no major change in the FGFET operating point. Thus, no major change in the steady state gate voltage occurs, and the drift created by the application of an input signal is greatly reduced over the circuit in Fig 20.

It has been indicated in a previous section how an

input field produces a transient change in the device operating point. This time varying component appears in the output of the field measurement circuit as a slow drift because the circuit output is directly related to the FGFET operating point. It is hoped that methods to reduce the effect of drift in the output can be applied.

The circuit in Fig 22 has the added advantage of having a very high gain. Small changes in Id, when multiplied by the resistance Ro, can result in a large voltage signal. Ro, representing $\Delta Vs/\Delta Id$, in this circuit may be the dynamic resistance of the transistor constant current source or some external resistance in parallel with this dynamic resistance. The dynamic resistance depends on the transistor used to implement the constant current source, but values on the order of tens of kilohms are possible. Experimental data presented in Fig 23 indicates the order of outputs over a range of inputs. Note that since the operating point of the FGFET does not change much when the input is applied, the output is nearly linear over a wide range of inputs - even though the FGFET is a nonlinear device.

The theoretical gain of the circuit can be estimated. The ratio of output change to change in input field is given by the change in drain current times the dynamic resistance at the constant current source.

$$\frac{\Delta V_s}{\Delta E} = \left(\frac{\Delta I_D}{\Delta E}\right) \cdot R_o \qquad (47)$$

The change in drain current with input field can be simply related to the parameters of the unmodified MOSFET by relating the input field to an equivalent change in gate voltage on an unmodified gate MOSFET, as in Eqn 46,

$$\Delta V_g = \frac{1}{\epsilon_r} \Delta E \cdot W \qquad (48)$$

where W is the distance separating the gate pad from the substrate. This distance is between 1000 and 2000 A for commercially available devices. Eqn (47) can be rewritten as

$$\frac{\Delta V_s}{\Delta E} = \left(\frac{\Delta I_D}{\Delta V_g}\right) \cdot R_o \cdot W \cdot \frac{1}{\epsilon_r} \qquad (49)$$

$\frac{\Delta I_D}{\Delta V_g}$ is a parameter often associated with unmodified MOSFETS and is termed the transconductance of the MOSFET, gm. The transconductance can be measured on a transistor curve tracer and is typically on the order of tens of mA/V. The theoretical magnitude of $\frac{\Delta V_s}{\Delta E}$ is on the order of

$$\frac{\Delta V_s}{\Delta E} \sim \left(\frac{10\,mA}{V}\right) * (10^4 \Omega) * (10^{-3} m)$$

$$\frac{\Delta V_s}{\Delta E} \sim \frac{10mV}{kV/m}$$

where ϵ_r has been ignored because it is on the order of unity. Experimentally, output signals of this order have been observed.

A practical problem associated with the high gain of this circuit configuration is establishing a workable operating point. If the drain to source voltage is fixed,

the amount of current that must flow through the device is determined by the I-V properties of the device. If the current demanded by the device is different from the current supplied by the current source, the difference in the currents must be made up by current flow through the resistor. Current flow through the resistor changes the source voltage. Since the circuit has a high gain, it takes very little current flowing through the resistance to cause the source voltage to become very large. Unless the drain to source voltage is set such that the current through the FGFET is nearly equal to the current supplied by the current source, large source voltages, that can saturate the elements in the actual circuit, will result. Thus, the establishment of an appropriate operating point is a practical problem that must be overcome.

This problem is compounded by the fact that the circuit must be at steady state to ascertain that an appropriate operating point has been established. When the value of drain to source voltage is changed, drift will occur as the circuit tends toward steady state and there is no certainty that a steady state operating point that does not saturate the circuit elements will be reached. Such a condition is unacceptable for the purpose of field measurement. A modified constant current source circuit that implements the voltage controlled current source is shown in Fig 22. This circuit allows the current source to be easily adjusted

so that by changing the control voltage its current matches the drain current flowing down from the FGFET. When no field is applied to FGFET, the circuit output should ideally be some fixed value that does not saturate any circuit element. Vcontrol can be adjusted based on Vs after the circuit approaches steady state following initial energization to ensure the bias output of the field measurement circuit reaches an appropriate value. This adjustment does not change the steady state operating point of the FGFET, just the output level, so it does not introduce any new transient changes in the output.

7 A SIMPLE SCHEME FOR DRIFT COMPENSATION

Characterization of the transient components of the FGFET operating point and knowledge of how these changes will be reflected in the output of the circuit using the FGFET to measure electric fields are both necessary before an attempt can be made to eliminate the transient components in the circuit output. In summary, transient changes in the FGFET operating point are first order exponentials with a time constant characteristic of the FGFET. All changes in the operating point produce output voltage signals that are linearly amplified representations of the change. Thus, at the output of the field measuring circuit, there will be a superposition of signals representing the transient changes in FGFET operating point, the instantaneous changes in operating point, and changes due to any applied field. Ideally, the transient components could be detected and measured, and then the output could be compensated to eliminate the affect of these drift components. The block diagram of a system to implement this function is shown in Fig 24. The success in eliminating the drift components from the output is directly related to how well they can be estimated.

Sophisticated techniques exist for detecting signals whose spectral densities are known.[2] Since the transients have been characterized as exponentials with time constants

on the order of hours, their spectral densiti
calculated. Fig 25 shows the spectral densi
exponential signal. Since the transient componen
output have a time constant on the order of ho
signals clearly are characterized by low frequenc
Fields to be measured would produce output compo
the same spectra as the input field. Fields tha
quickly in comparison to the drift would hav
densities characterized by high frequencies, and th
be very little overlap in the frequency domain of
field signal and the drift. Thus, it seems possible
drift in the output could be approximately det
measuring only the low frequency components in th
Low pass filtering of the output gives an estimati
drift.

A low pass filter whose output would be an es
the drift is required to have a cutoff frequency l
that it does not pass components of the input field
enough that all of the drift components are passed.
real signals are not sufficiently band limited suc
appropriate cutoff can be selected without compromi
or both, of these requirements. In this way, the
far from optimal, but if a large part of the d
signal outputs are separated far enough in frequ
imperfect estimate of the drift can still imp
accuracy of field measurements.

A cutoff frequency that causes most of the drift to be passed means that most of the energy of the drift signal is passed. By integrating the energy density function in Fig 25, it is seen that the exponential function, which has been shown to represent the drift components in the output, has a finite total energy given by [10]

$$\int_0^\infty |X(\Omega)|^2 d\Omega = \int_0^\infty \frac{1}{\Omega^2 + \frac{1}{\tau^2}} d\Omega = \frac{\pi}{2}\tau \text{ joules}$$

where Ω represents analog frequency in rad/sec. Though the exact choice of a good cutoff frequency is dependant on the sense in which good is defined, one possible criterion is that 90% of the total energy in the drift signal is contained in frequencies below the cutoff frequency. This frequency, Ω_c, can be determined by straightforward calculation

$$\int_0^{\Omega_c} \frac{1}{\Omega^2 + \frac{1}{\tau^2}} d\Omega = 90\% \cdot \frac{\pi}{2}\tau$$

Solving for yields

$$\Omega_c = \frac{6.314}{\tau}$$

Expressed in Hertz, this cutoff would be about $\frac{1}{\tau}$ Hz. Data on time constants for the FGFET shows that this cutoff could be on the order of several thousandths of a Hertz. Implementation of an analog filter with a cutoff frequency on this order would be cumbersome. However, a digital filter with a cutoff this low is easily implemented. A generally

accepted procedure for the design of digital filters is presented in reference [9]. The calculations for a first order filter are contained in Appendix 2. These calculations show that a simple first order filter has a difference equation

$$y(n) = x(n) + b_1 x(n-1) - a_1 y(n-1)$$

Appendix 3 describes the hardware needed to implement the filter and interface it to the field measuring circuit.

Fig 26 shows the measured and theoretical frequency response of the implemented digital filter designed to have a cutoff on the order of hours. (Note that it is a simple matter to change the cutoff frequecy since it may be varied by changing the filter constants in the digital program.) Fig 27 shows how well the filter measures the drift at the output of the FGFET sensor system with no signal applied, and Fig 28 shows the response of the system in response to a step input in field.

7.1 Shortcomings of Lowpass Filtering

Experimental data obtained using a digitally implemented lowpass filter and shown in Fig 27 and Fig 28 reveal shortcomings in this technique used for estimating drift. As evidenced in Fig 27, the lowpass filter has a time lag between input and output. There are two reasons for this

lag. First, low pass filters intrinsically have phase responses such that a delay is introduced between input and output signals. This problem is inherent to lowpass filters in general. The phase lag will increase as the cutoff frequency is lowered. In other words, this time lag can be considered to be a result of not all the frequency components of the drift being passed by the filter. The experimental data in Fig 27 shows the output of a filter with a low cutoff frequency and the delay is evident. Thus, a higher cutoff would include more of the actual drift components in the estimate of the drift provided by the filter output, but could adversely affect the system performence in measuring an electric field by erroneously including more of the signal components in the estimate of the drift.

Secondly, there is a form of delay associated with the quantization of the input signal by the A/D which must precede the digital filter. The output of the A/D and thus the filter input can only change in discrete steps of one least sign[illegible]ant bit. In Fig 29, it can be seen the the A/D input mu[illegible]e from V1 to V2 before the A/D output reflects a[illegible]ange in the input voltage. If the input is varying slowly, the time difference, T2-T1, may be very large, and there would be a significant delay before the filter could begin to respond to any changes in the input between T1 and T2. This quantization delay varies inversely

with the change in input voltage represented by one least significant bit at the A/D output. This type of delay must be considered in the design of hardware to implement the lowpass filter.

Another problem with this technique for separating true signal from drift can be seen by examining the system response to a step input. (Fig 28) In this case, the frequency components of the input field are not well separated from the frequency components that are being interpreted by the system as part of the drift. Thus, even though there is little or no change in the input, the system overestimates the drift by including the low frequency components of the signal in the estimate of the drift. The overestimate of drift occured in this example to an appreciable degree, even though the cutoff frequency of the filter was on the order of hours. The output of the system shown in Fig 24, then, represents the ideal output reduced by the amount of the overestimation of the drift.

In addition, low pass filtering is sensitive to changes that occur over a long period of time. Such things as changes in component values, changes in amplifier gains, or deviations in fixed sources will all be reflected in the output of the low pass filter. Such changes must be guarded against in the design of hardware systems to implement the low pass filter.

7.2 Recomendation

The lowpass filtering technique for separating drift from signal can be effective in cases where the drift and input field signal are widely separated in the frequency domain. However, this technique exhibits major shortcomings when slowly varying fields are to be measured.

It is important to note, though, that the changes in the FGFET operating point have been characterized based on a physical model of the device, and experimental data confirms that this is an accurate characterization. The application of more sophisticated methods of detecting drift may possibly be applied successfully to separate drift from input even when the signal has many low frequency components.

7.3 Status

As of this writting, the hardware for a system to compensate for the drift in the output of the FGFET detector circuit using lowpass filtering to estimate the drift has been built and tested. The system was tested using various values of cutoff frequency for the digital filter, which is implemented in software and may be easily modified for cutoff frequency. A first order filter with a time constant (reciprocal of cutoff frequency) was shown to be able to track output drift very well, but with this cutoff the low

frequency components of input signals simulating fields that might be measured by the device in actual space applications were included in the estimate of the drift made by the filter.

One way to judge how much of the signal is included in the estimate of the drift is to apply an unchanging input to the filter. The longer the input is applied, the lower the frequency components of the signal are. For example, a constant input applied to the filter for fifteen minutes would have lower frequency components than a constant input applied for only five minutes. Thus, an informal figure of merit for any filter, implemented in software here, would be the length of time a constant input could be measured without the filter seriously overestimating the drift by including the low frequency components of the signal in the estimate of the drift. With the filter time constant of fifteen minutes, constant inputs could be measured for only a few minutes.

It is desired that this sensor system eventually be able to measure fields that are nearly constant for a period of time of an hour or more. Work is continuing at Boston University's High Voltage Laboratory to determine if a suitable filter time constant can be found to make measurements of this type possible. Future systems will include circuits to prevent some types of instantaneous changes in FGFET operating point from occuring. Variations

in room temperaure over the course of a day or from day to day have been observed to be large enough to produce significant changes in FGFET operating point, so temperature variations will be tightly controlled. This additional control will make it easier to estimate the drift for two reasons. First, when factors that produce instantaneous changes are limited, the drift in the circuit output is smaller since these instantaneous changes give rise to drift. Secondly, temperature variations, even though they appear in the circuit output as soon as they occur, produce what seems to be drift because the changes in temperature occur, in most instances, as slowly as the drift. Controlling the temperature is thus another way to reduce slow changes in the circuit output. By reducing the magnitude of the drift, the estimate of the drift, though still delayed at the filter output, would differ from the actual drift by a smaller amount. If techniques are simultaneously used to reduce the drift, the cutoff frequency can be lowered, increasing the delay between the true drift and the filter's estimate of the drift without increasing the magnitude of the overall error in estimating the drift. In this situation, it may be possible to lower the cutoff frequency enough to measure input signals that are nearly constant for an hour or more.

Work on this project is scheduled to continue at BUHVL with the goal of developing a sensor system that is capable

of measuring slowly varying electric fields.

8 SUMMARY

Factors that affect the FGFET operating point have been investigated. A model that predicts device operation compatable with experimental observation has been developed. Using this model, the changes in operating point have become better understood. Moreover, a certain class of changes in device operating point have been shown to be first order exponentials.

With the understanding of the FGFET operation gained in this investigation, a simple method for reducing the affects of changes in FGFET operating point has been formulated, and its shortcomings and advantages have been discussed. Though no definitive solution to the problem of FGFET operating point drift was found, the characterization of the nature and origin of this drift is neccessary groundwork for more practical, effective methods of compensation.

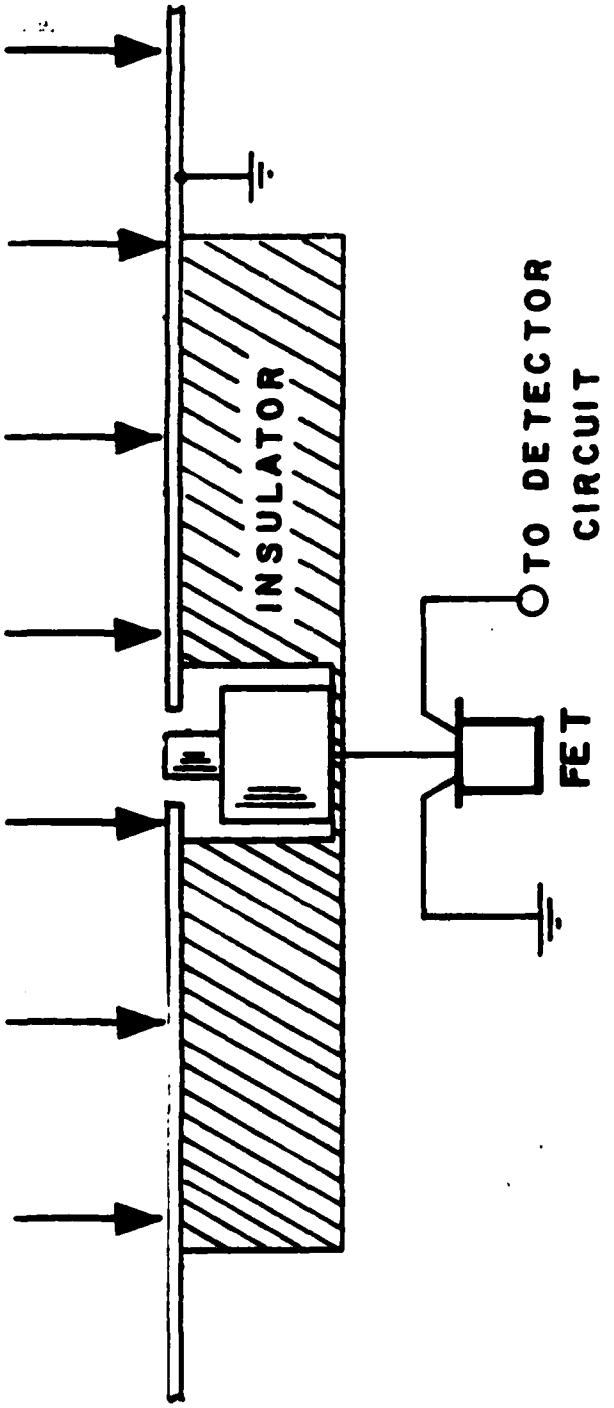


Fig 1 Field measurement scheme using an unmodified MOSFET.

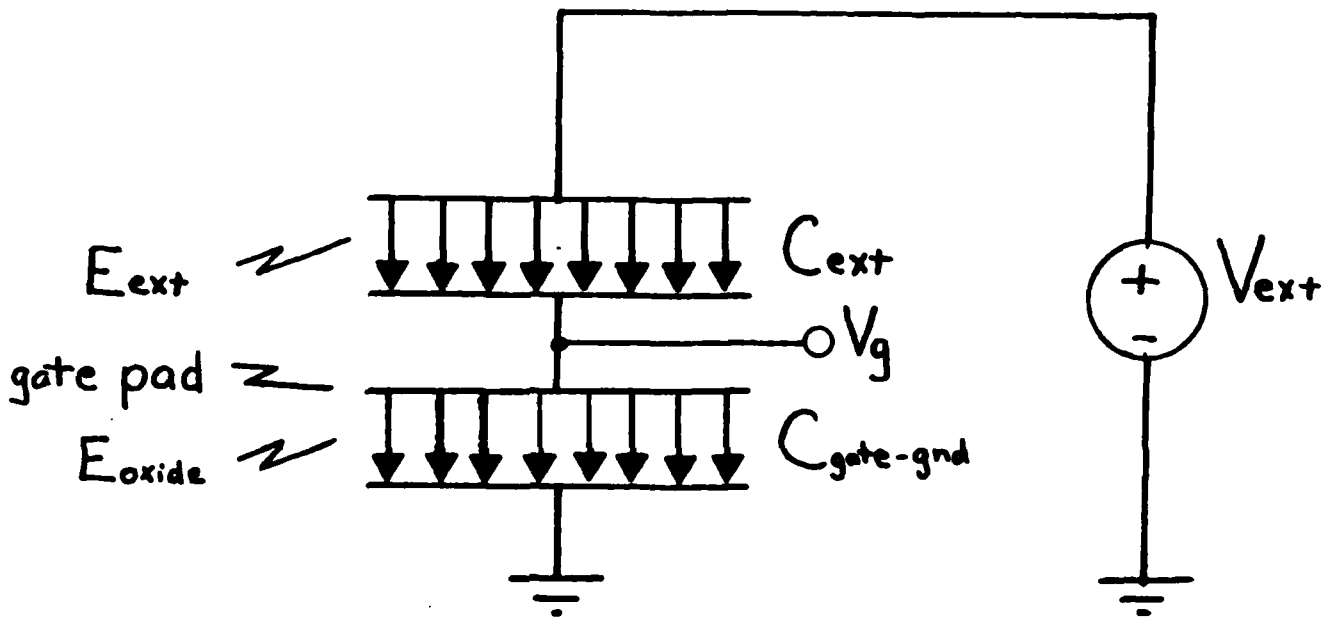


Fig 2 Model of capacitive coupling of FET to an external field, which is represented by Cext and the voltage source Vext.

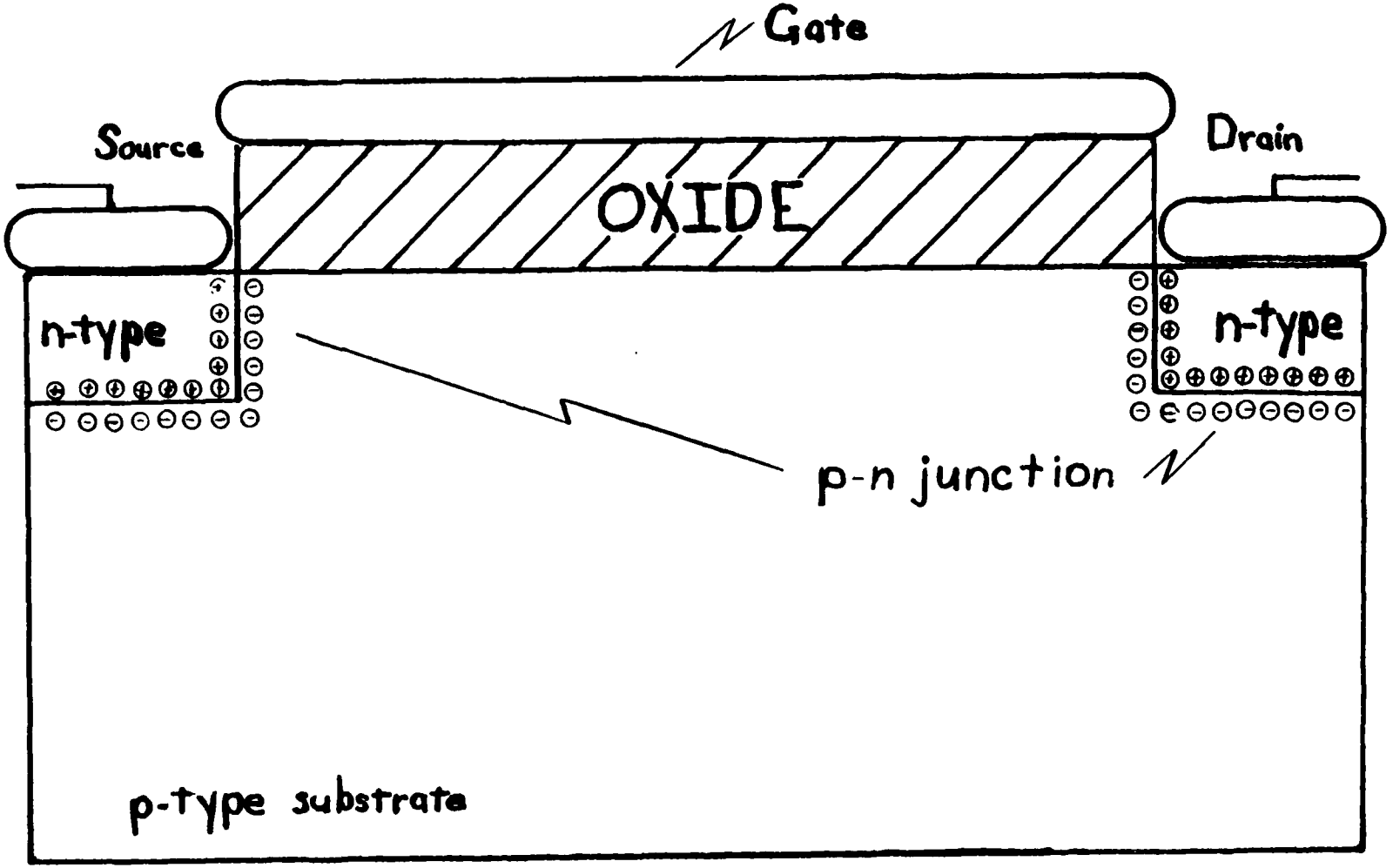


Fig 3 Simplified FGFET geometry.

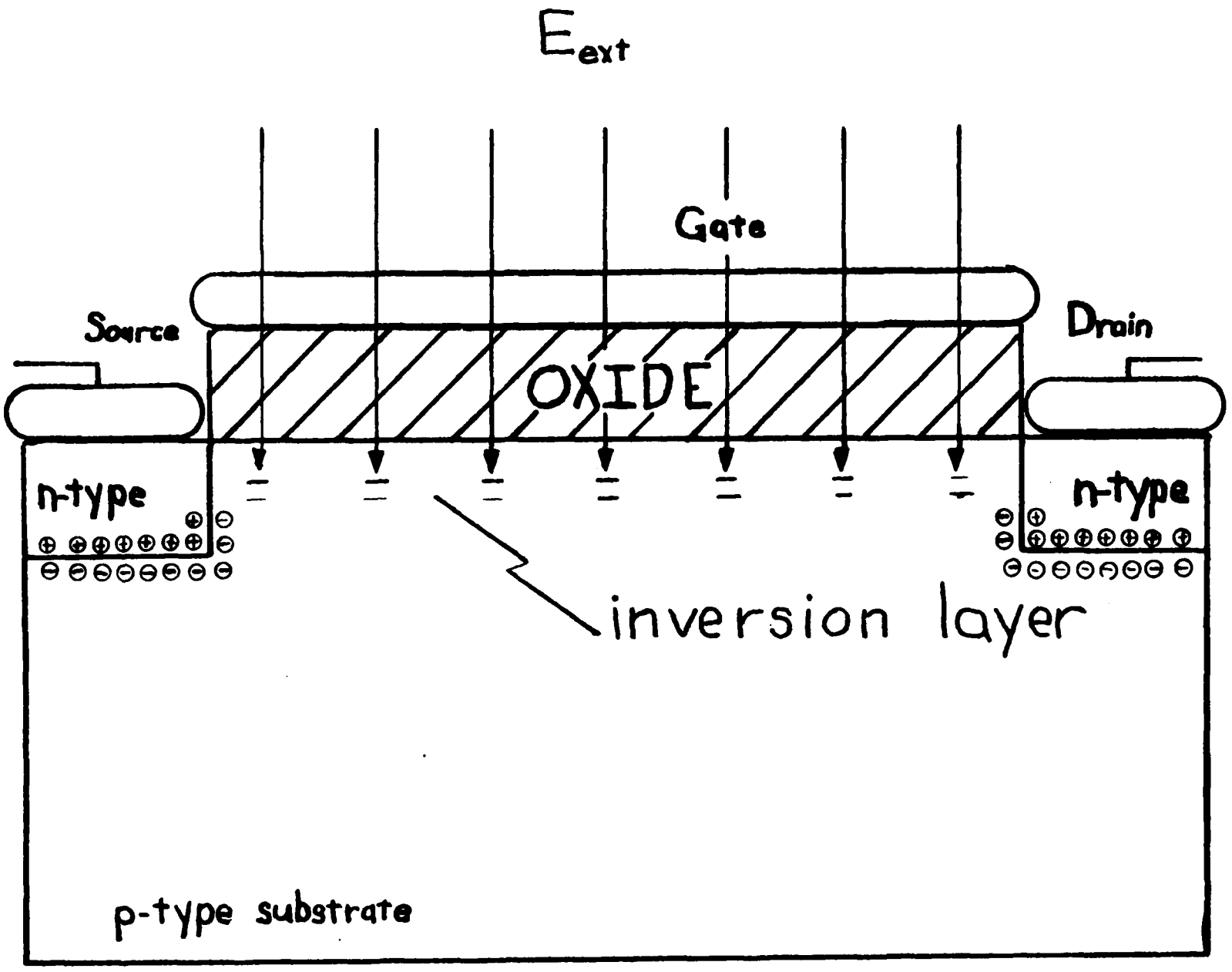
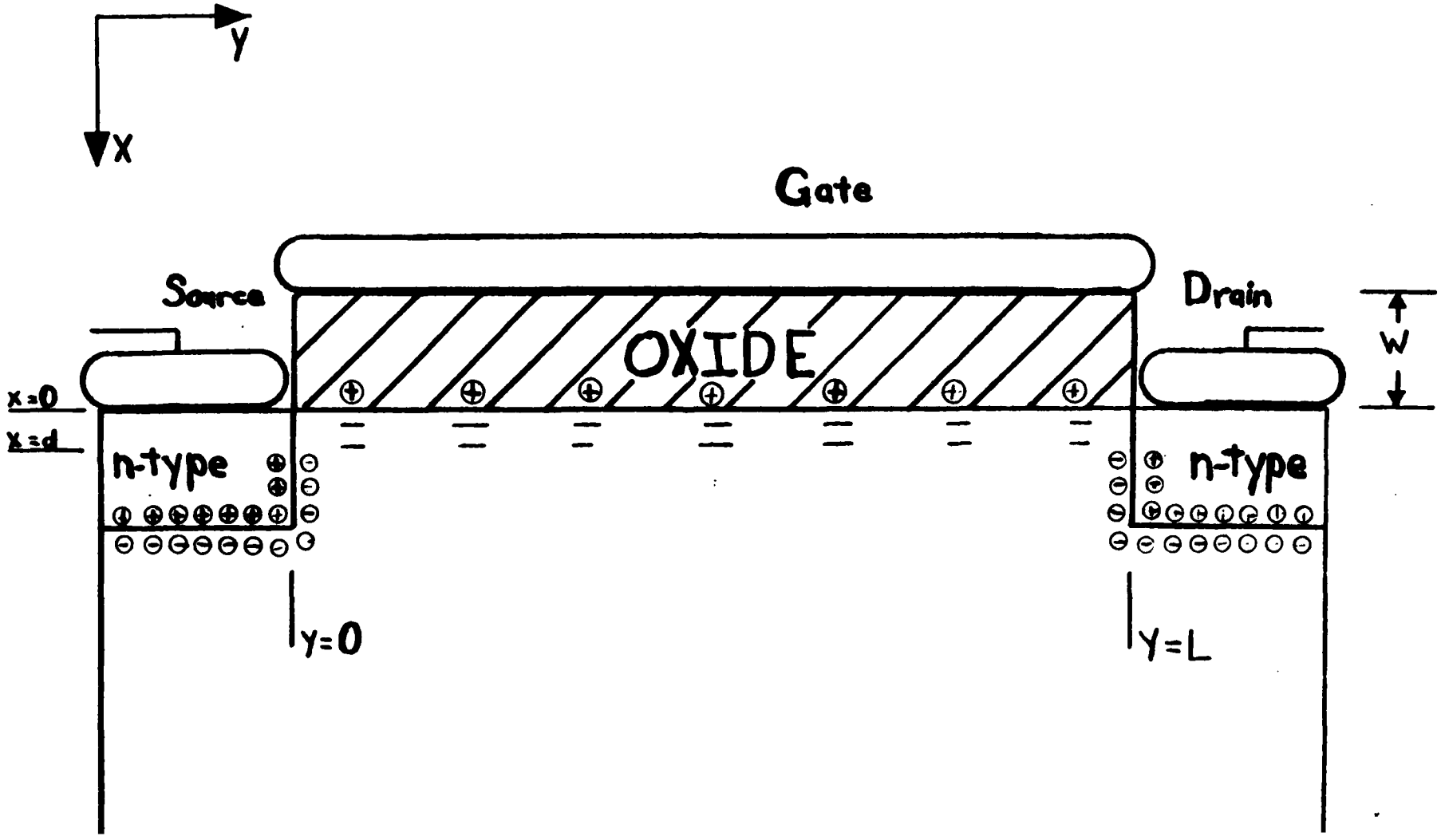


Fig 4 FGFET with an inversion layer induced by an external field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OXIDE
W
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x=d
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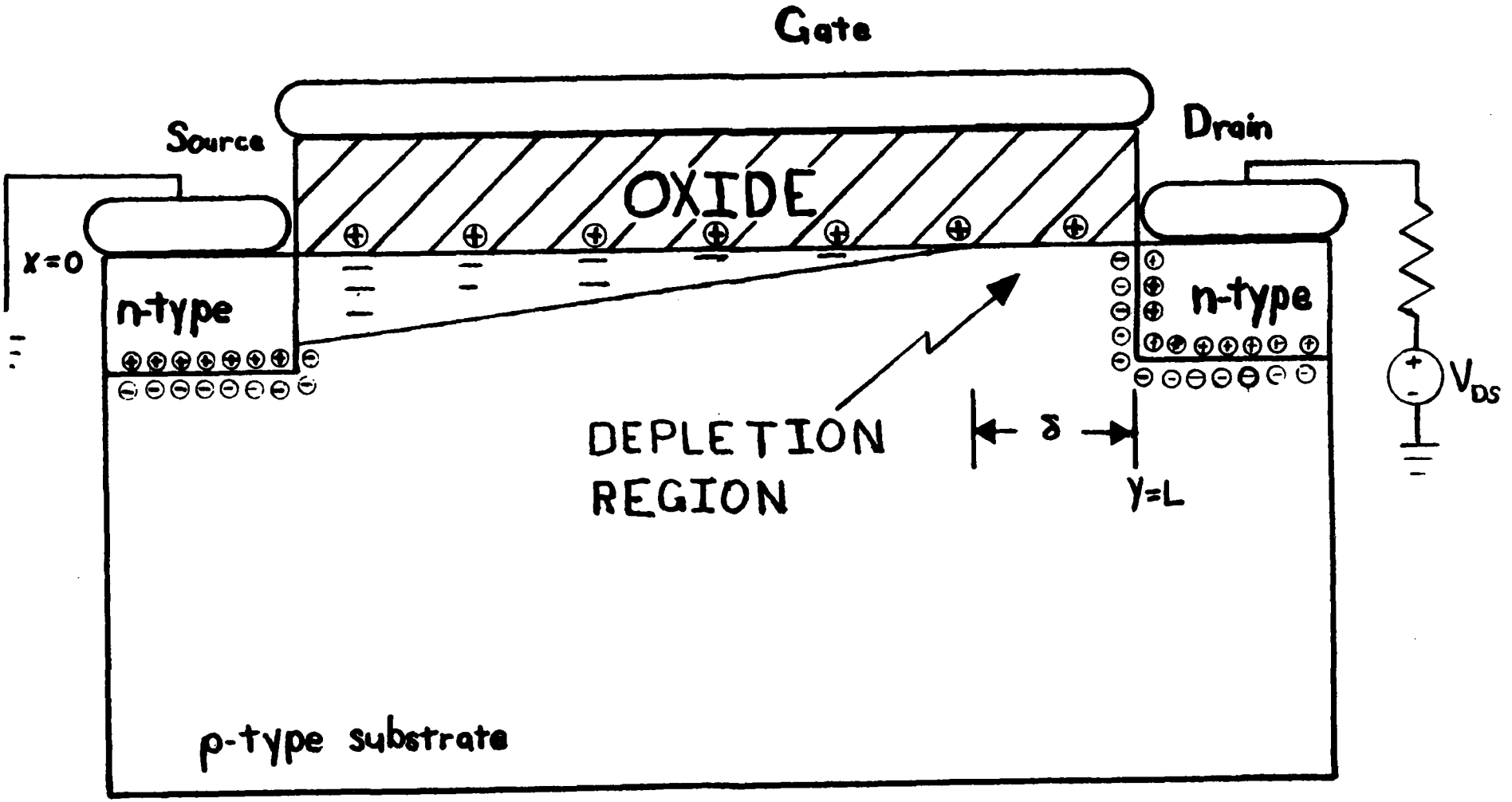


Fig 6 FGFET with inversion layer and depletion region formed when Vds> Vg-Vp

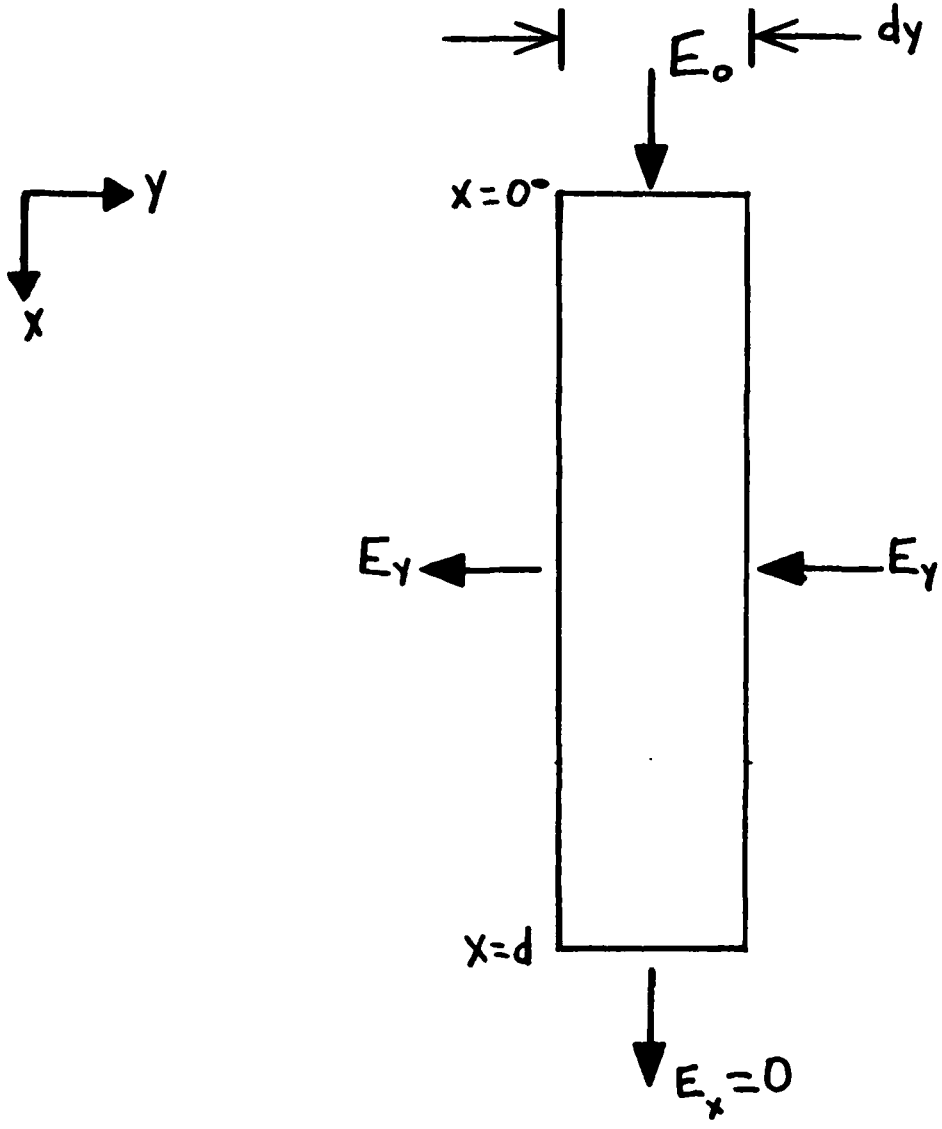


Fig 7 A differential slice of the FGFET channel showing the approximate field values used to calculate the divergance in the channel

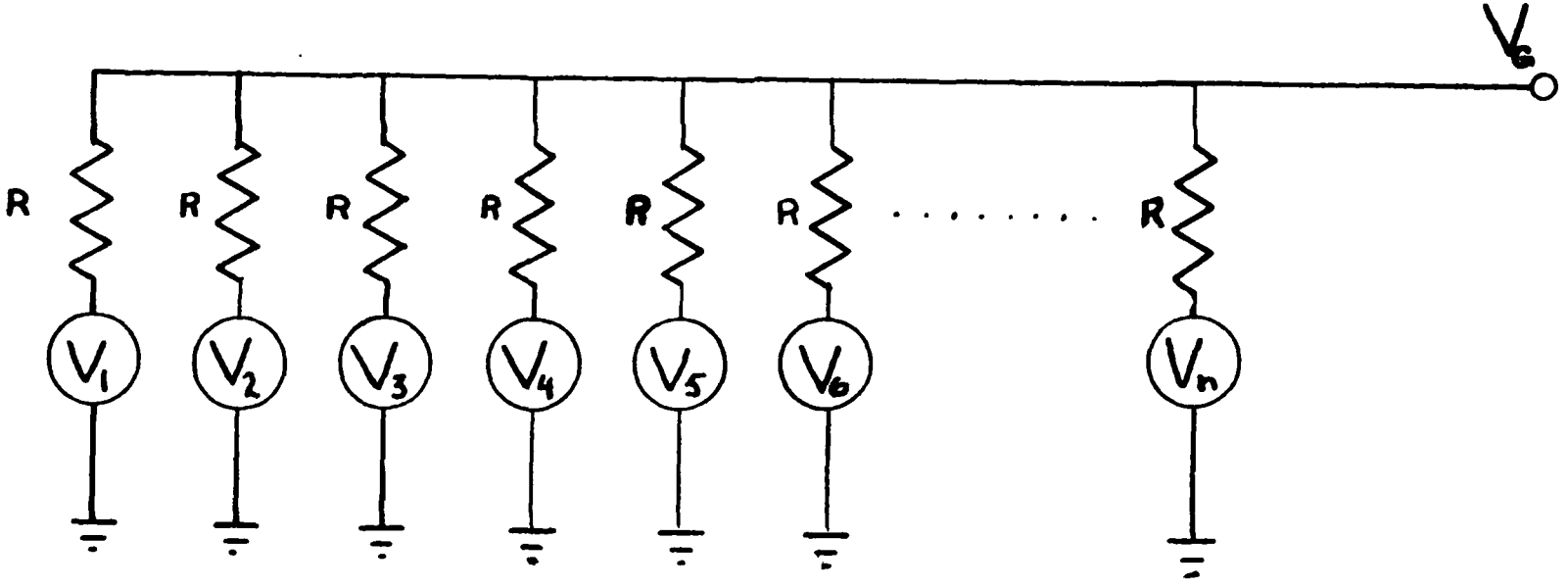


Fig 8 Model of linking of voltage distribution in channel to the gate pad
The resistors represent the oxide layer and the voltage sources represent the voltage along the channel. Each voltage source may be different, but the resistors are the same.

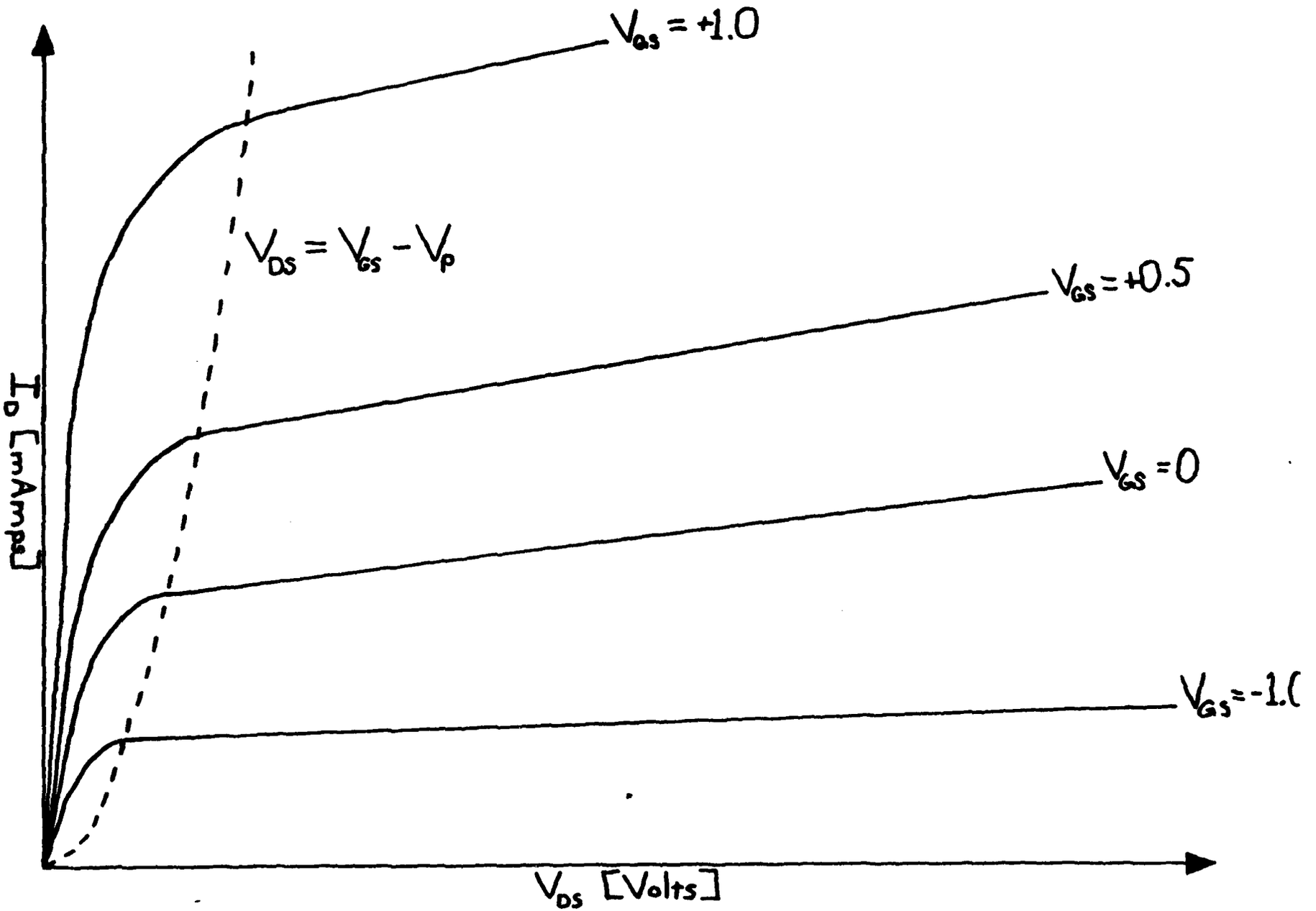


Fig 9 I-V curve of an unmodified MOSFET

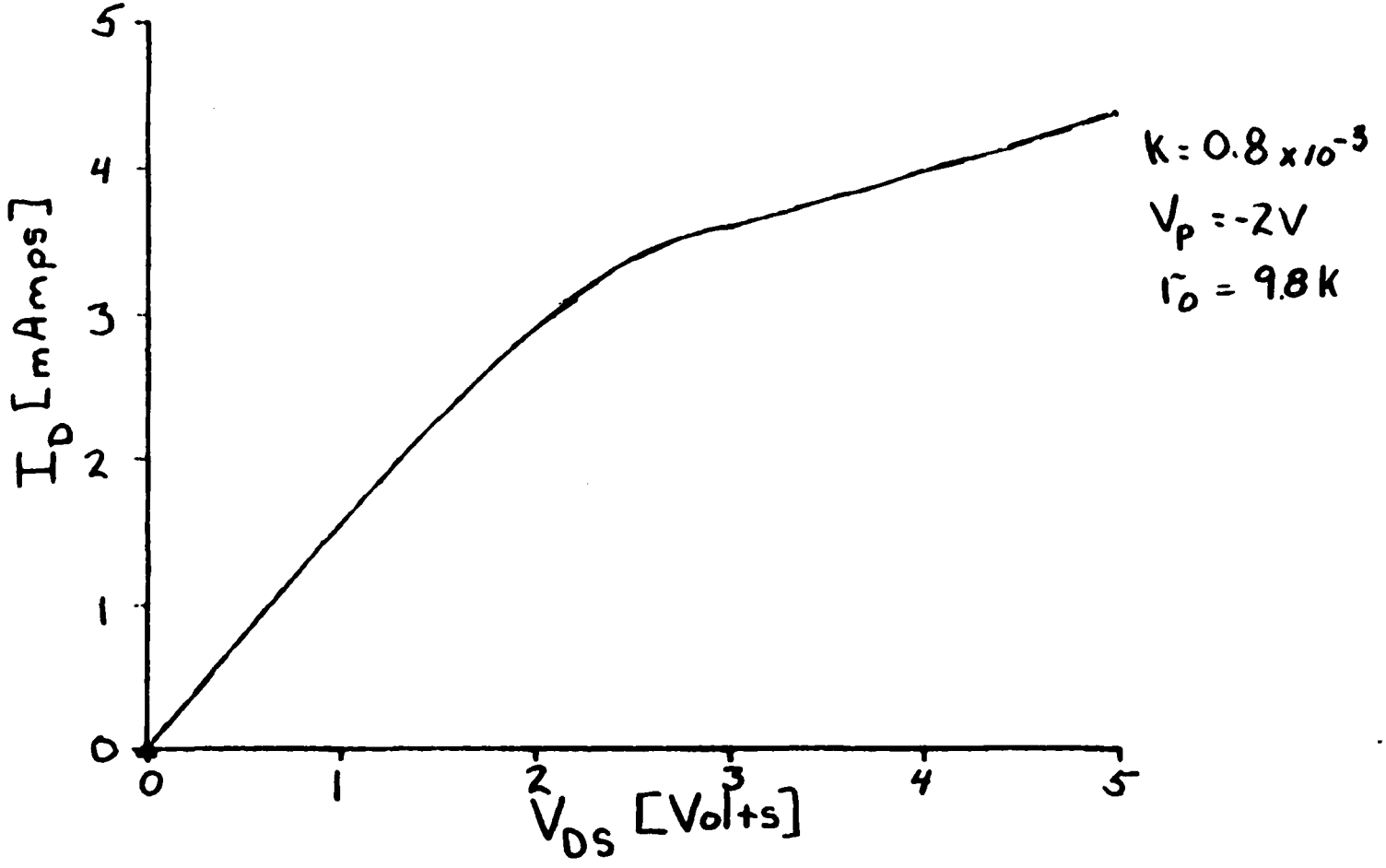


Fig 10 Predicted FGFET I-V plot from solution of Eqns 18, 22, 24 and 32, 41, 42

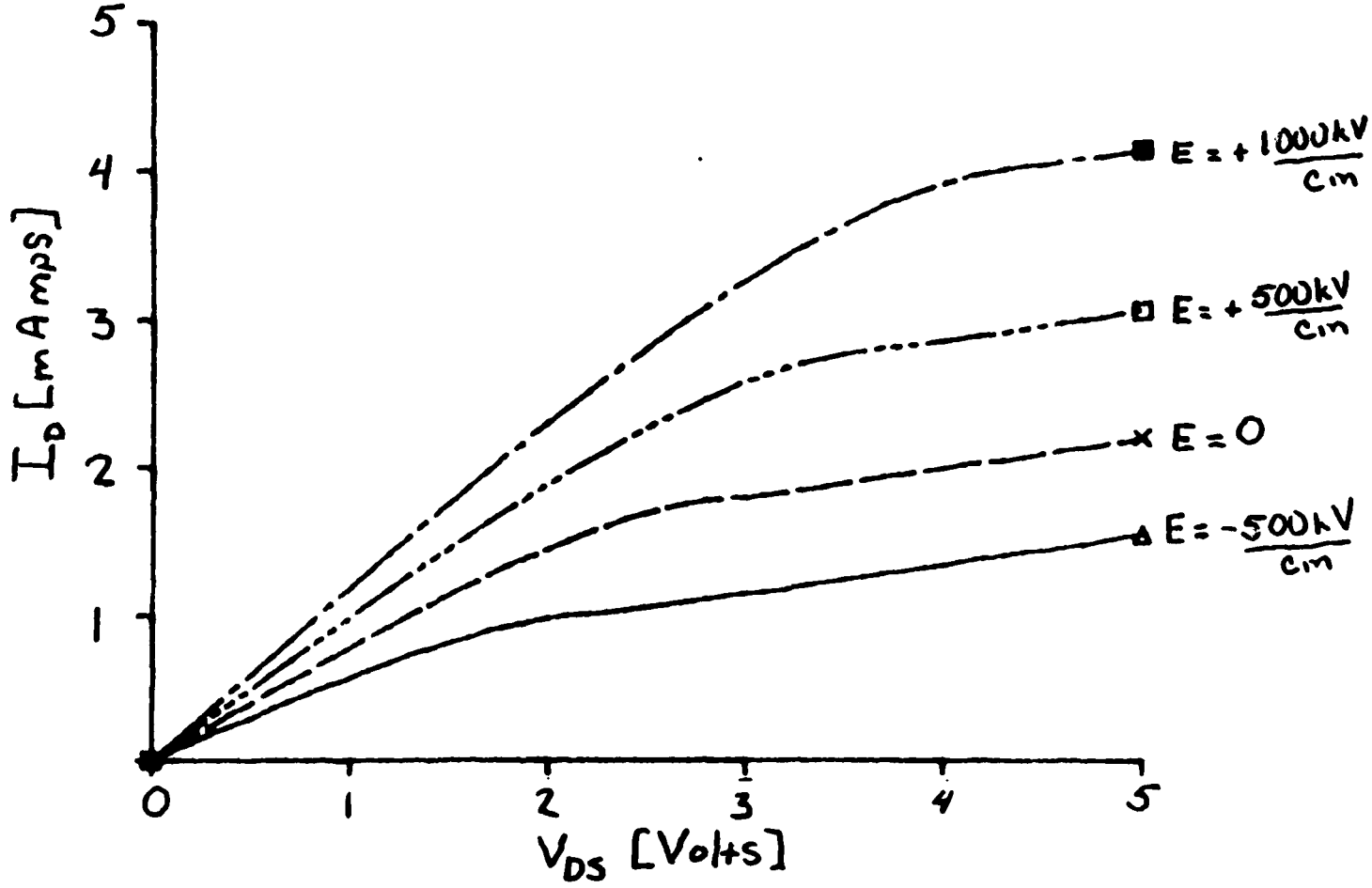


Fig 11 Effect of applied field on FGFET operating characteristics
Notice the appled fields are several orders of magnitude larger than could practically be applied to illustrate the changes.

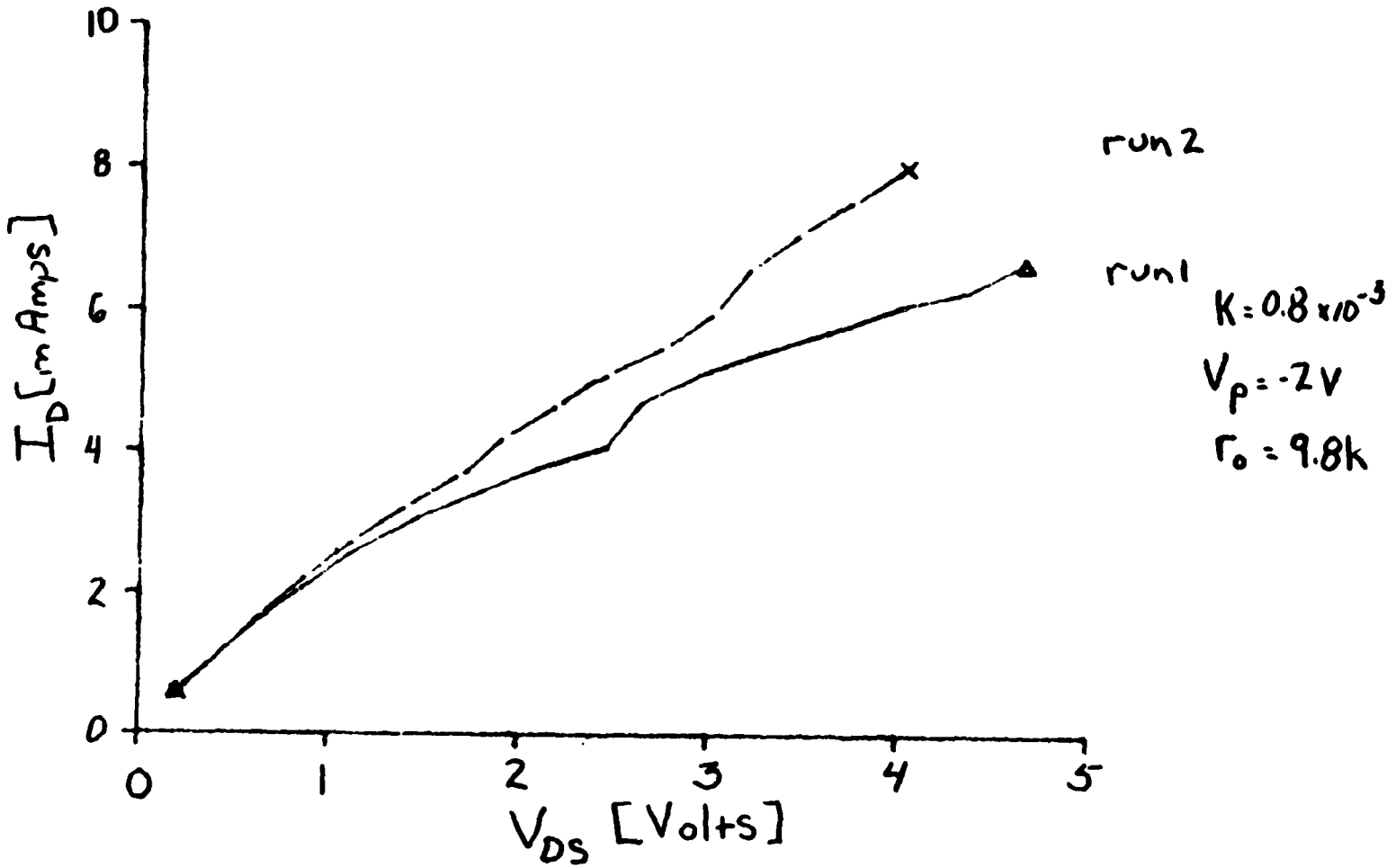


Fig 12 Experimental data of FGFET operating characteristics

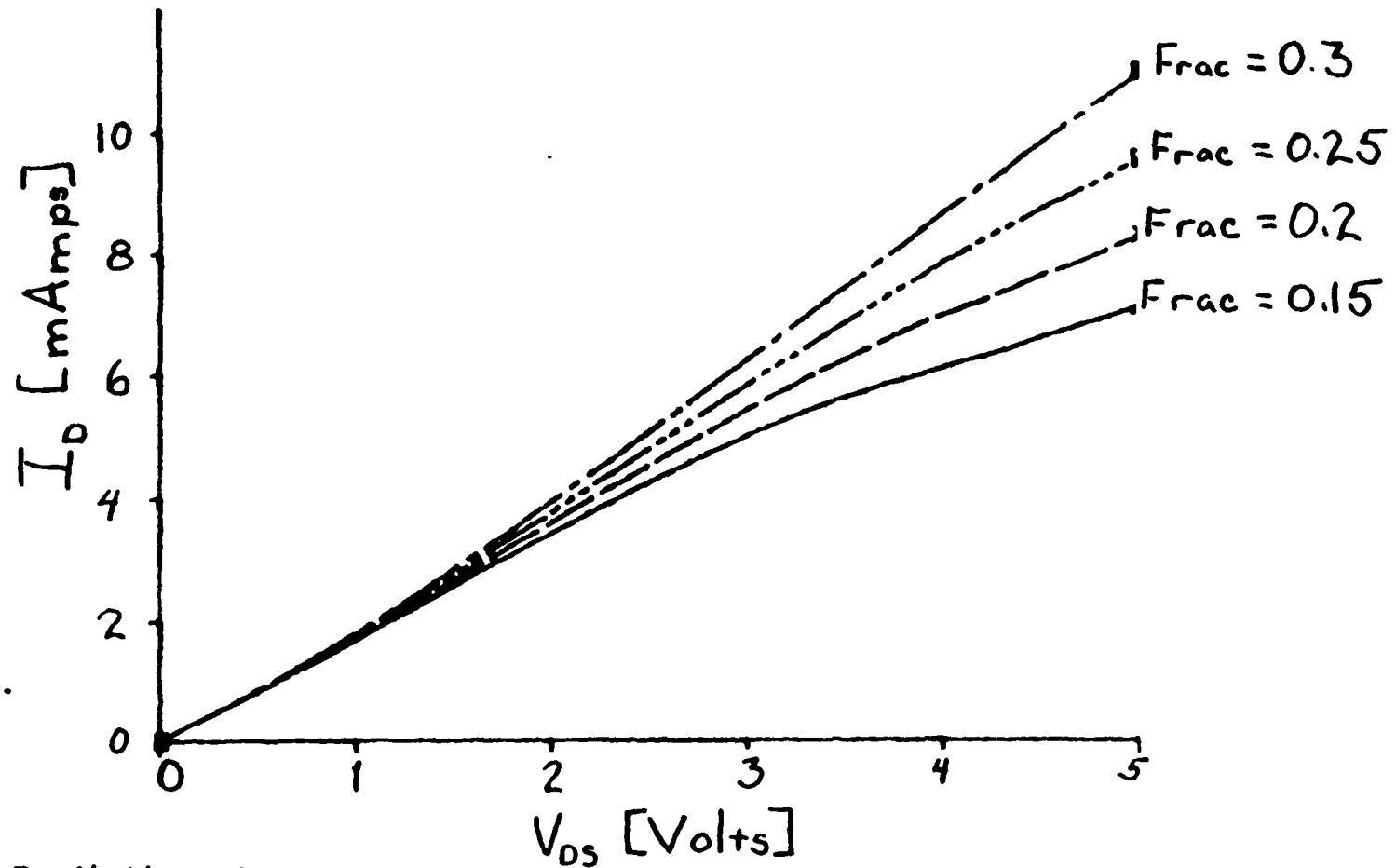


Fig 13 Prediction of FGFET operating characteristics including linking between drain and gate and gate and source. "Frac" tells the fraction of the drain to source voltage linked to the gate.

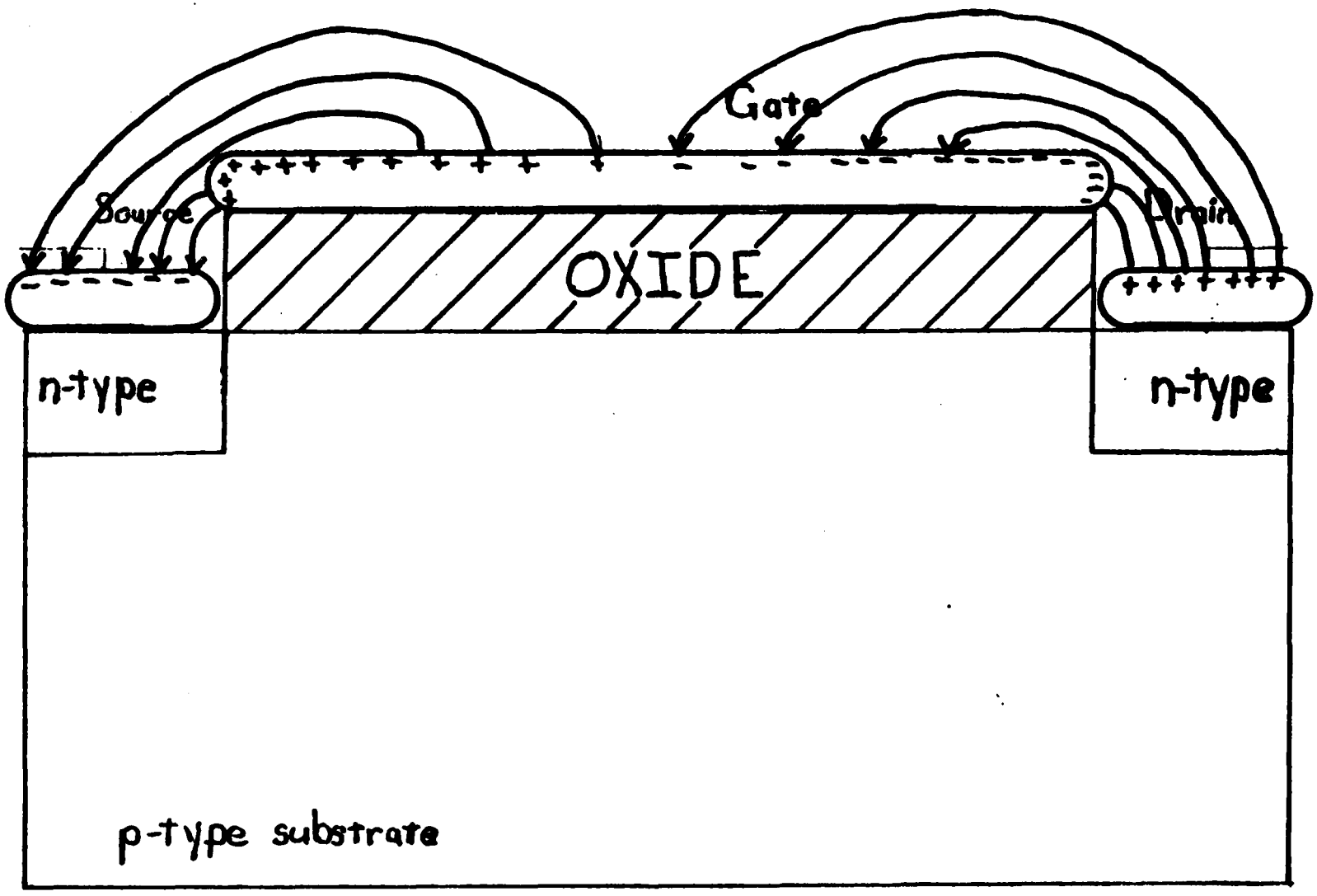


Fig 14 Schematic view of gate pad charge and field pattern after a drain to source voltage is applied

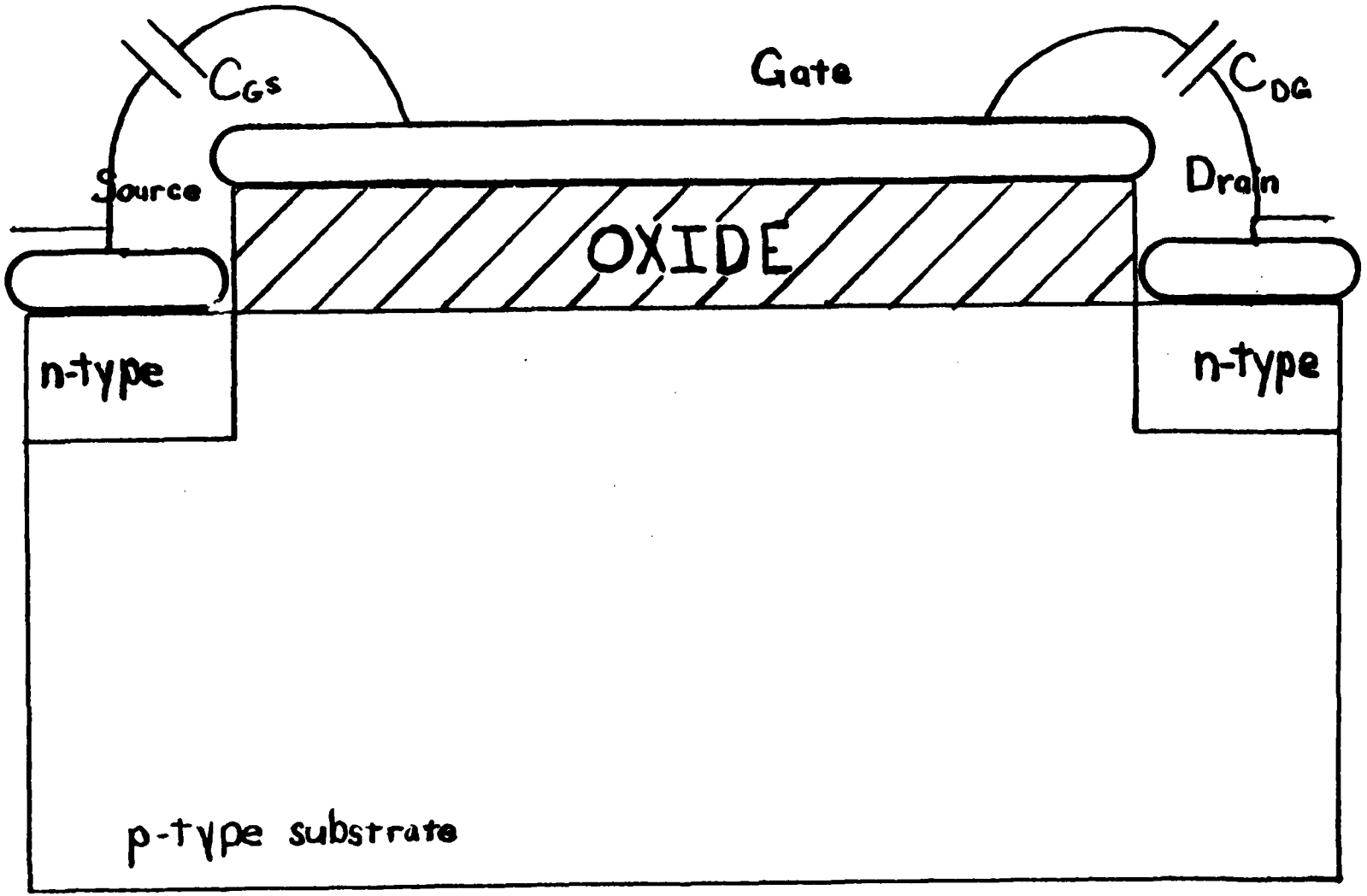


Fig 15 Lumped capacitance model of fields linking gate, drain, and source

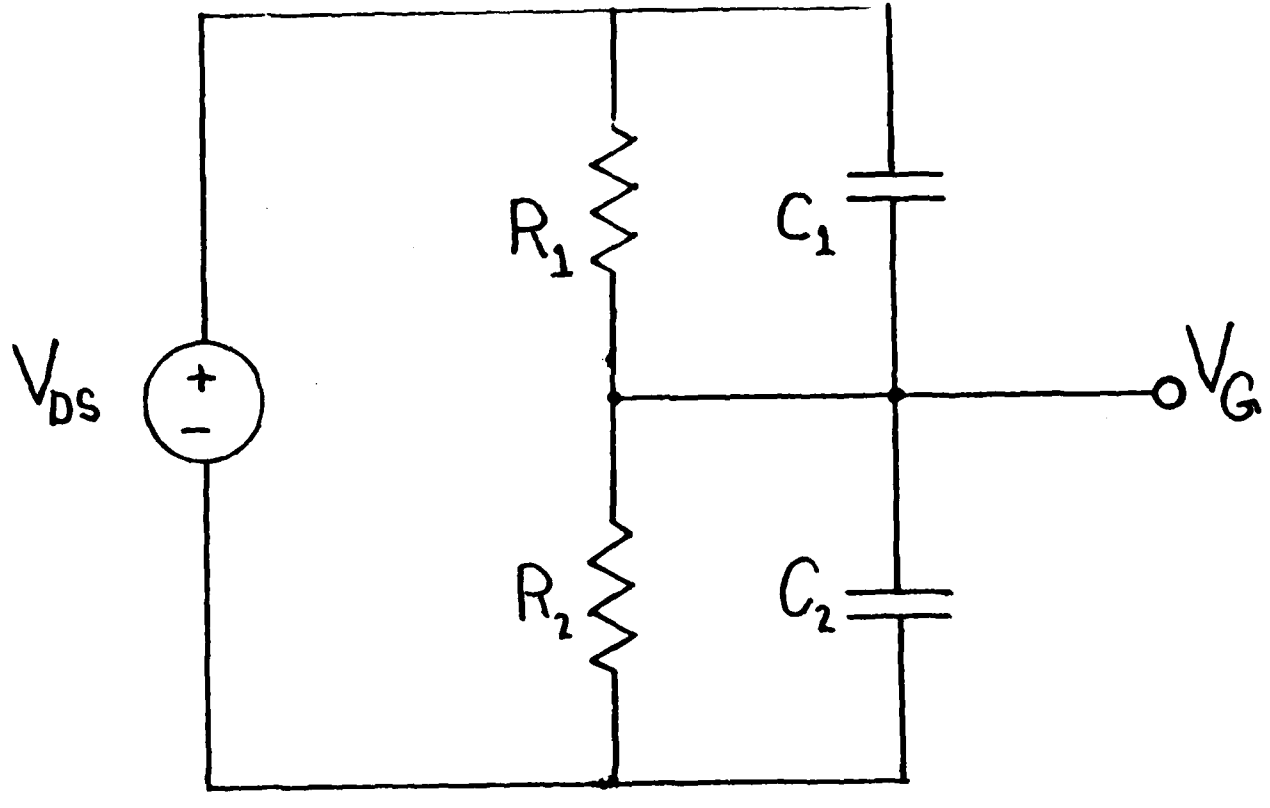


Fig 16 Model of all linking to gate pad. C1 and C2 are drain to gate and gate to source capacitances, respectively. R1 and R2 represent the conglomeration of all resistive linking to the gate pad: surface paths from drain and source, and paths through the oxide layer to the substrate.

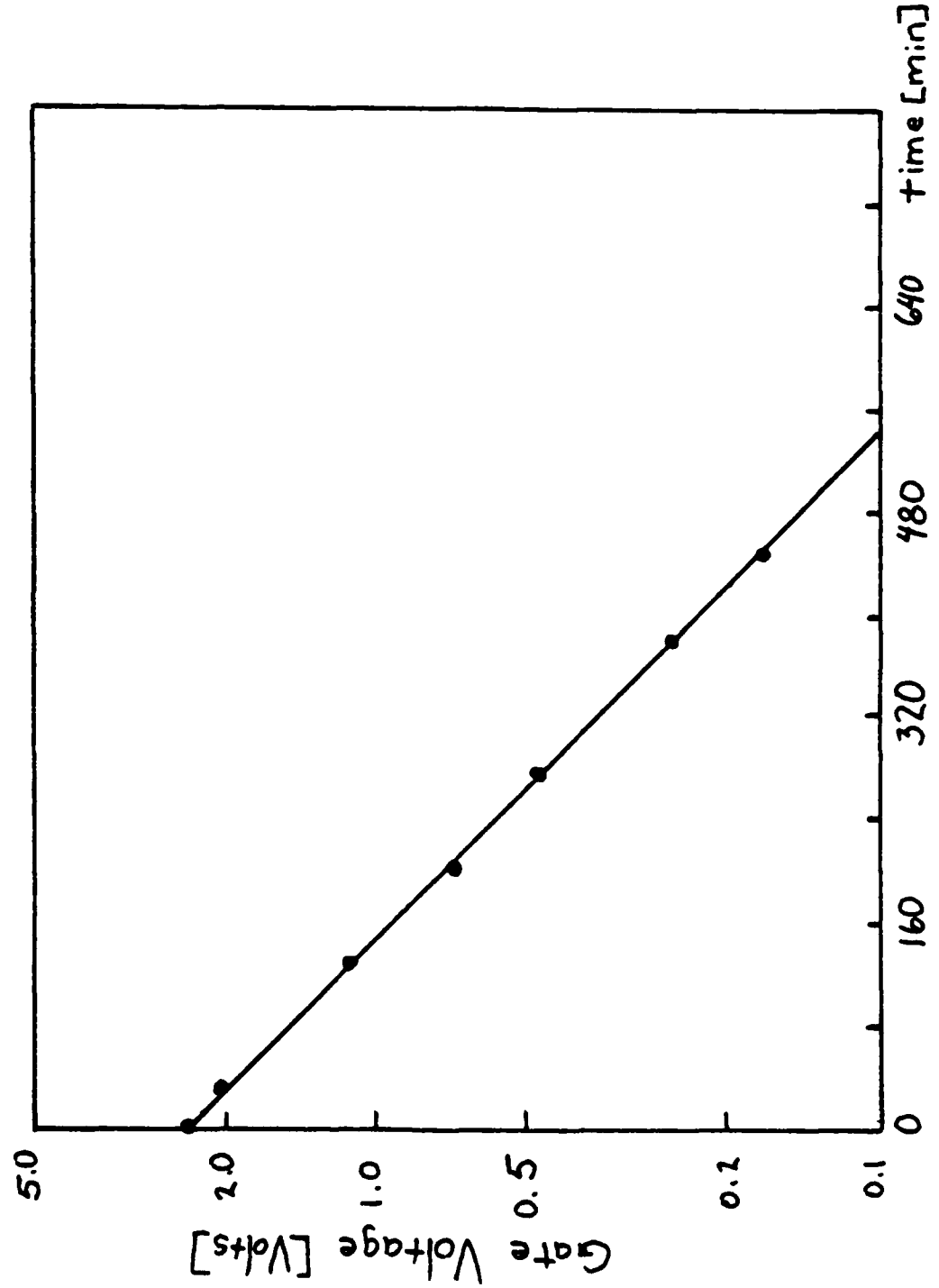


Fig 17 Experimental data showing decay of gate voltage in response to a step input in Vds

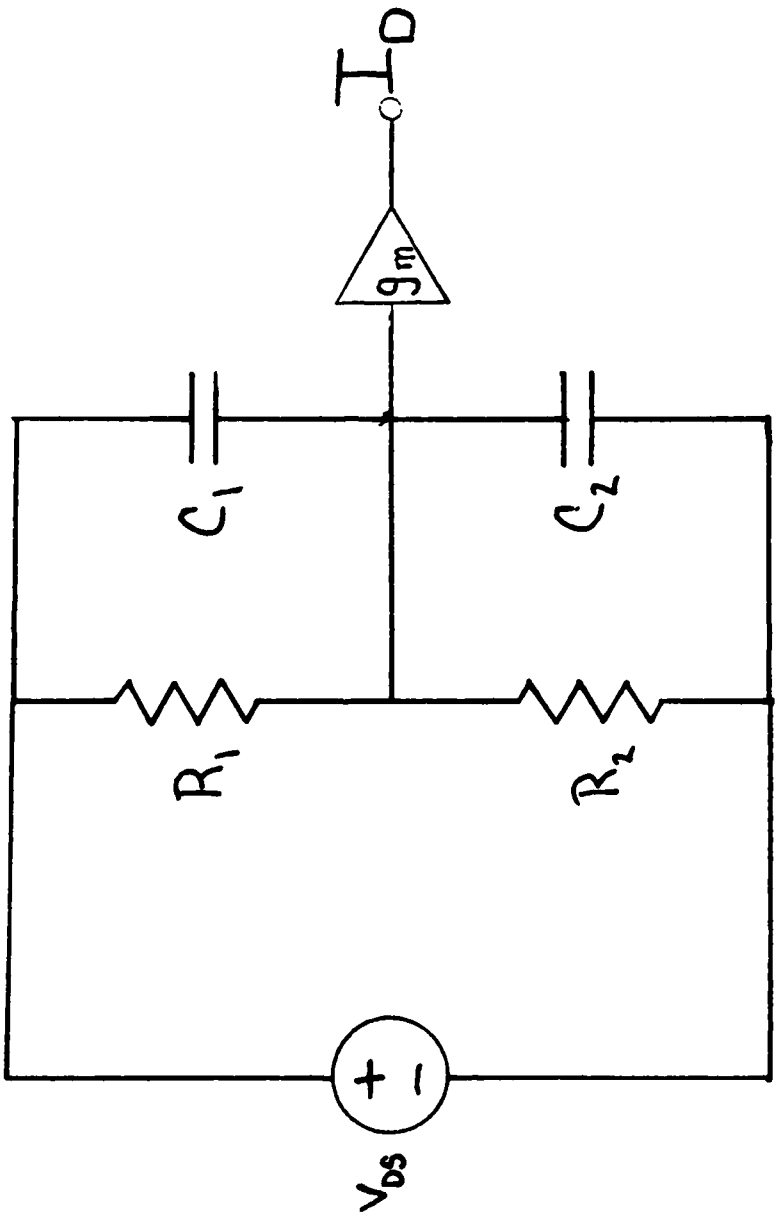
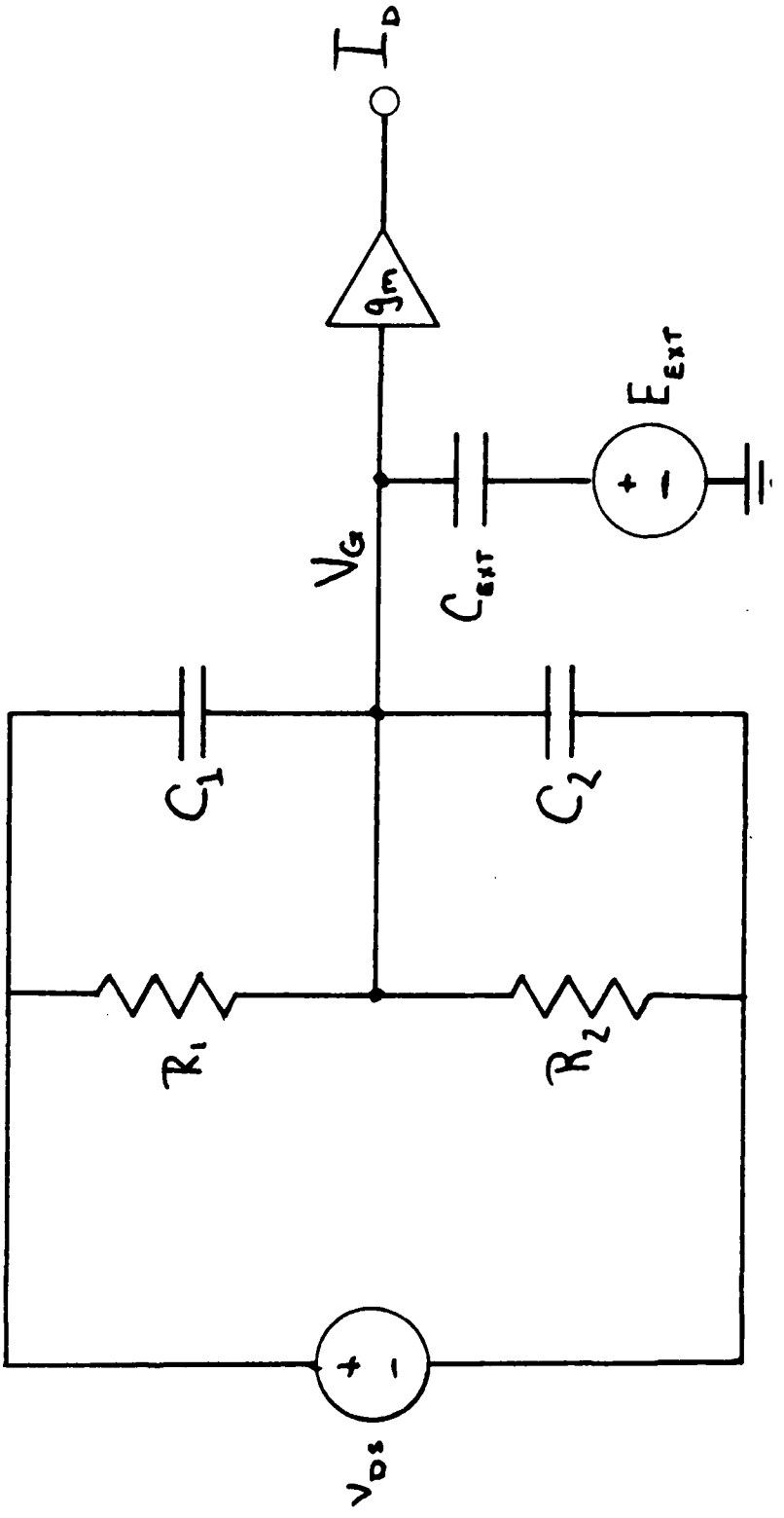


Fig 18 FGFET incremental model for small changes around a given gate voltage


I_D
g_m
E_{EXT}
V_G
C_{EXT}
C_1
C_2
R_1
R_2
V_{DS}

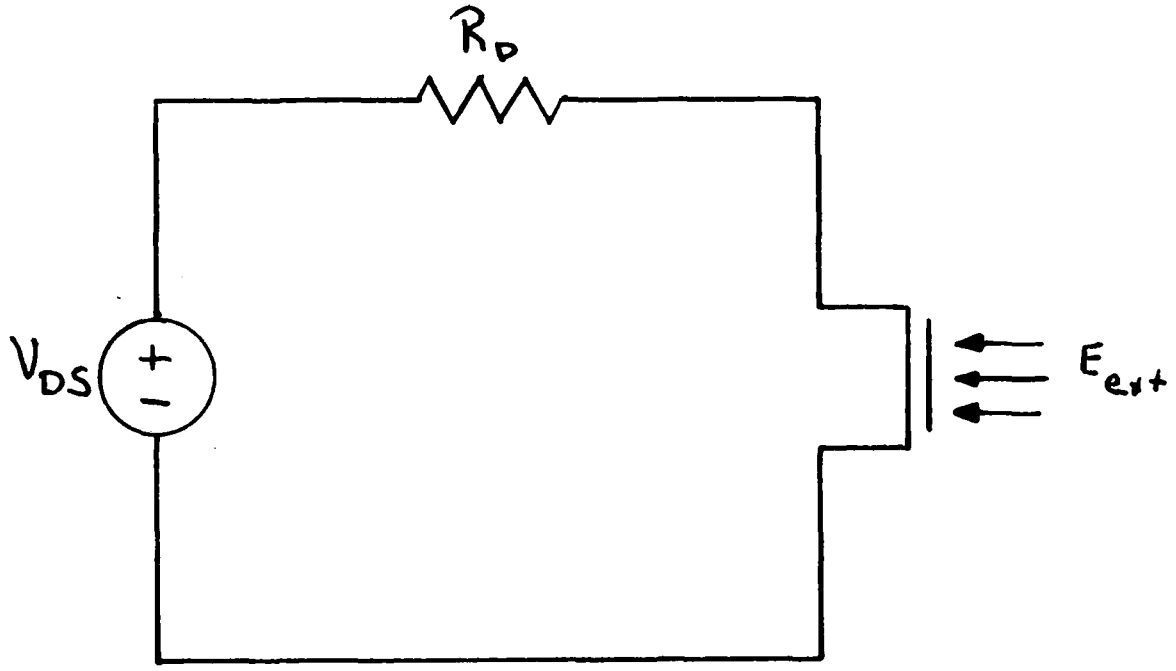


Fig 20 A simple circuit using an FGFET as a field sensor

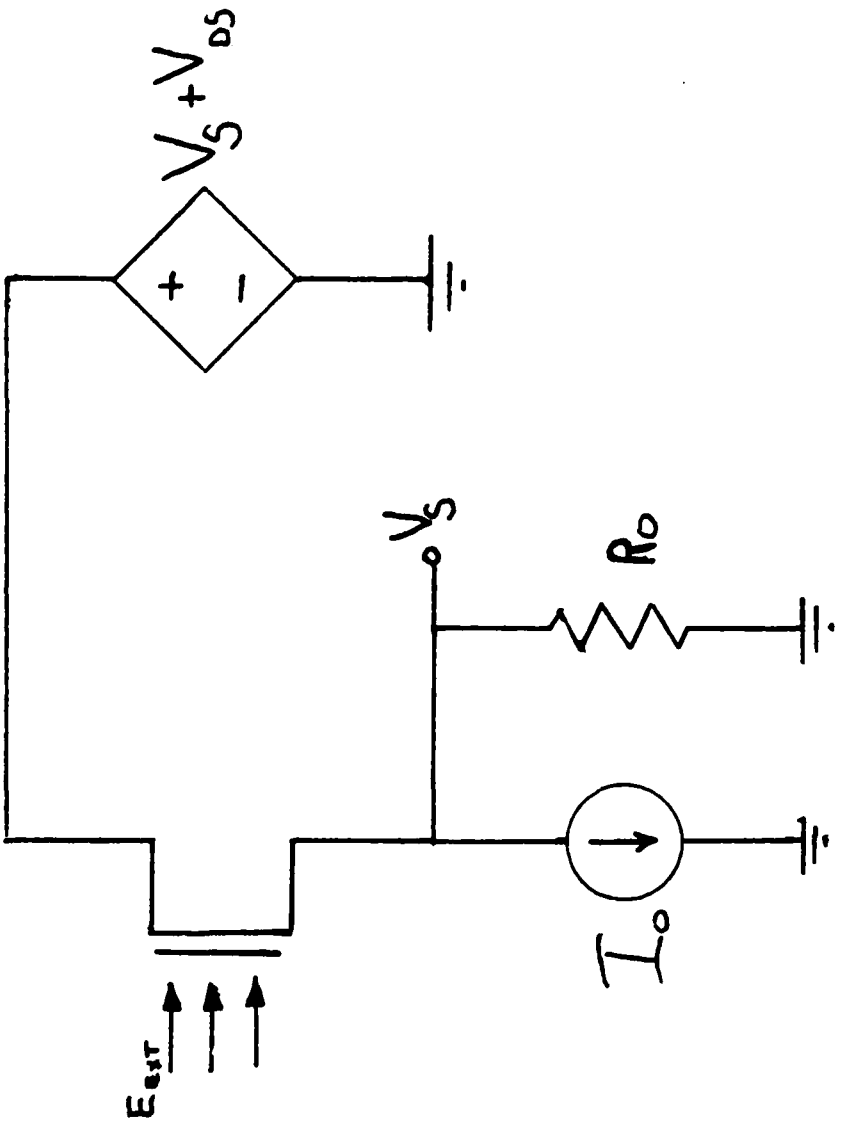


Fig 21 Model of an improved circuit using the FGFET as a field sensor The drain to source voltage is constant, regardless of output.

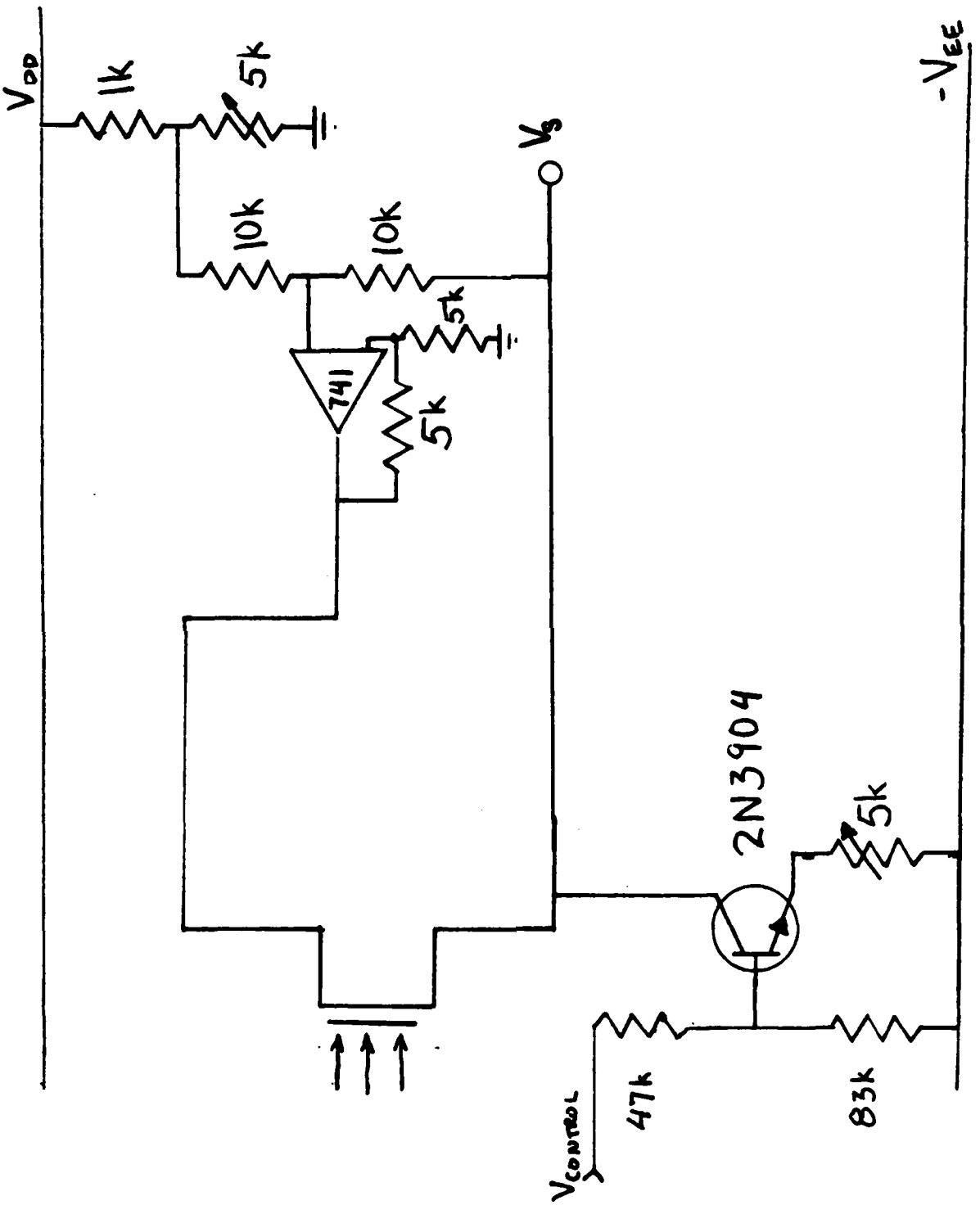


Fig 22 Improved circuit using FGFET as a field sensor

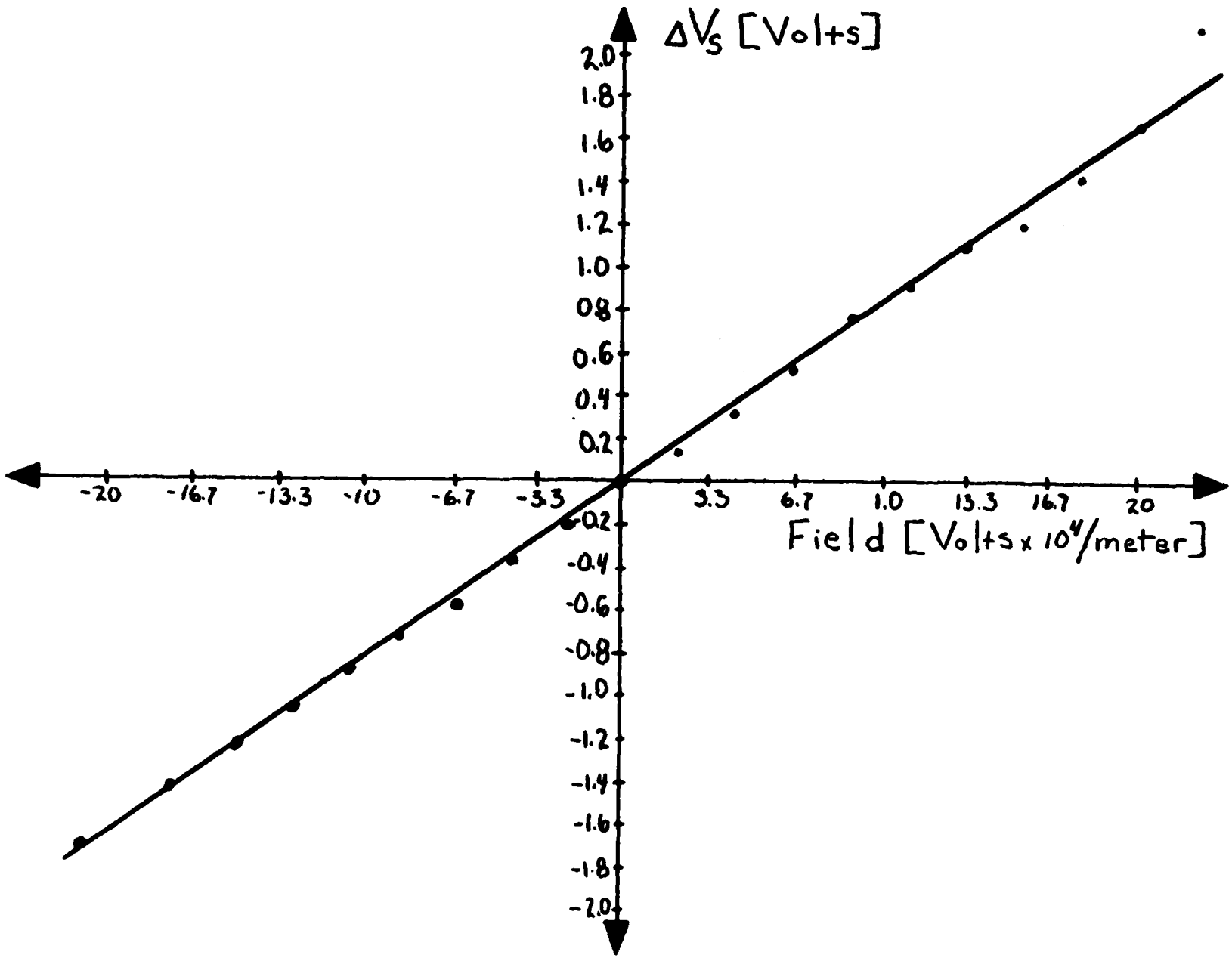


Fig 23 Output of FGFET detector circuit in response to an input field

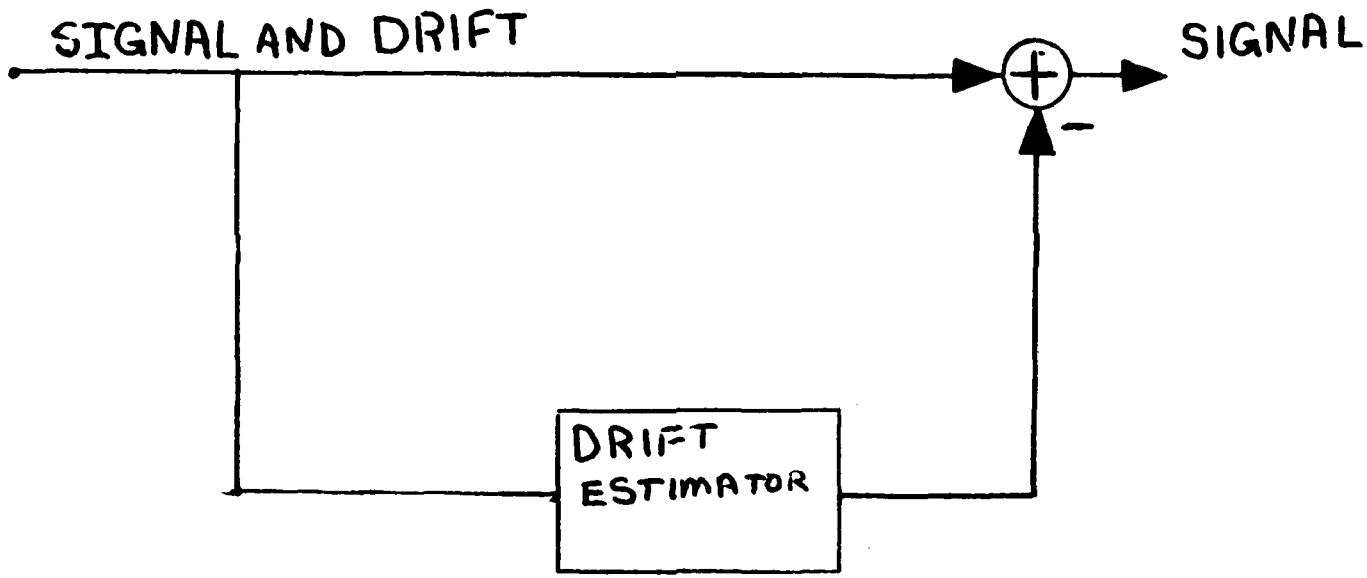


Fig 24 Block diagram of a system to correct for drift in FGFET field sensor circuit

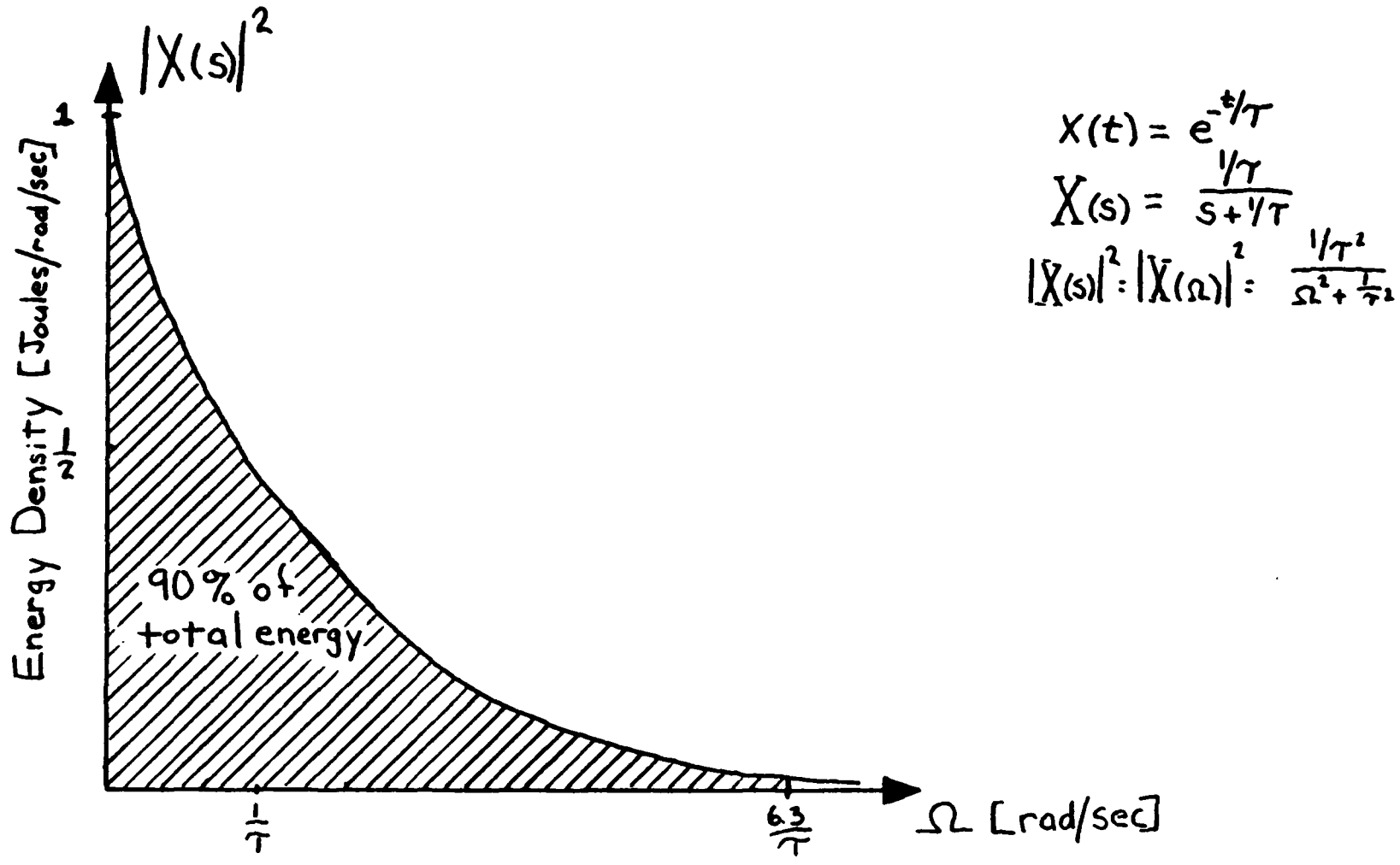


Fig 25 Energy density function of an exponential signal, which is used to represent the drift in the output of the FGFET field sensing circuit
Ω is used here to represent frequency in rad/sec.

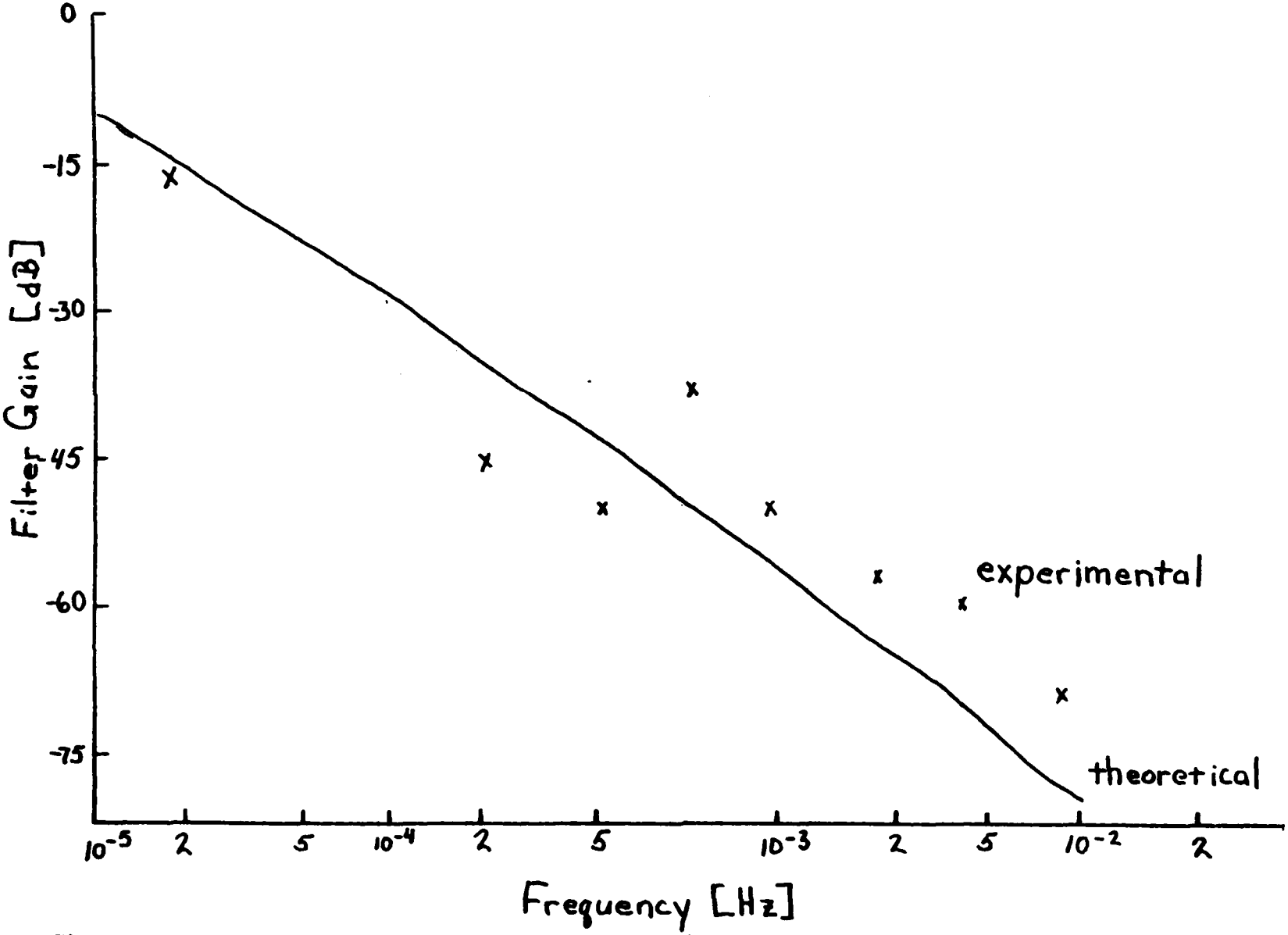


Fig 26 Frequency response of first order digital filter with a time constant on the order of hours. This filter has 0dB gain at dc.

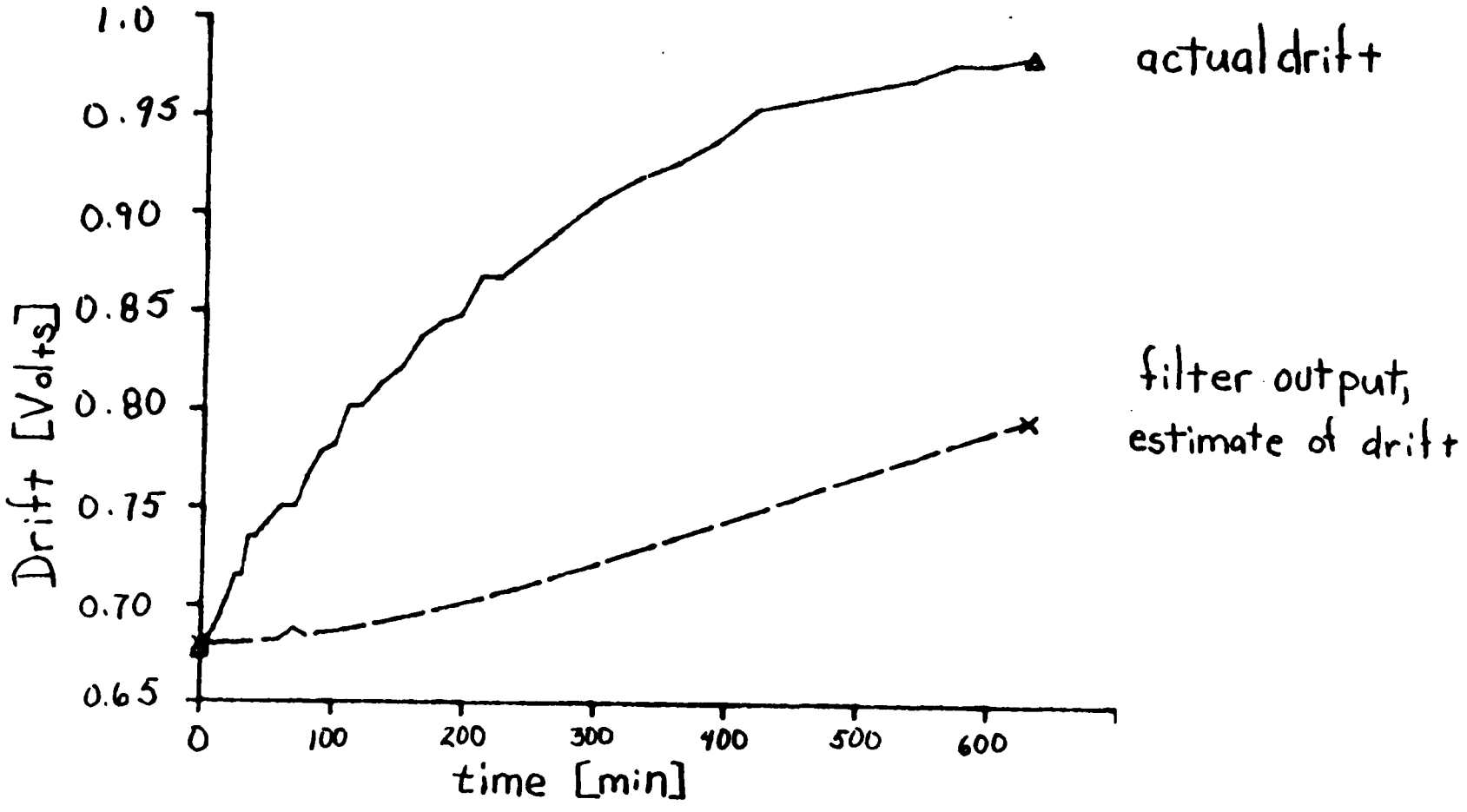


Fig 27 Illustration of how a low cutoff frequency, on the order of hours, affects the filter's estimate of the drift. The difference between the two curves represents an underestimate of the drift.

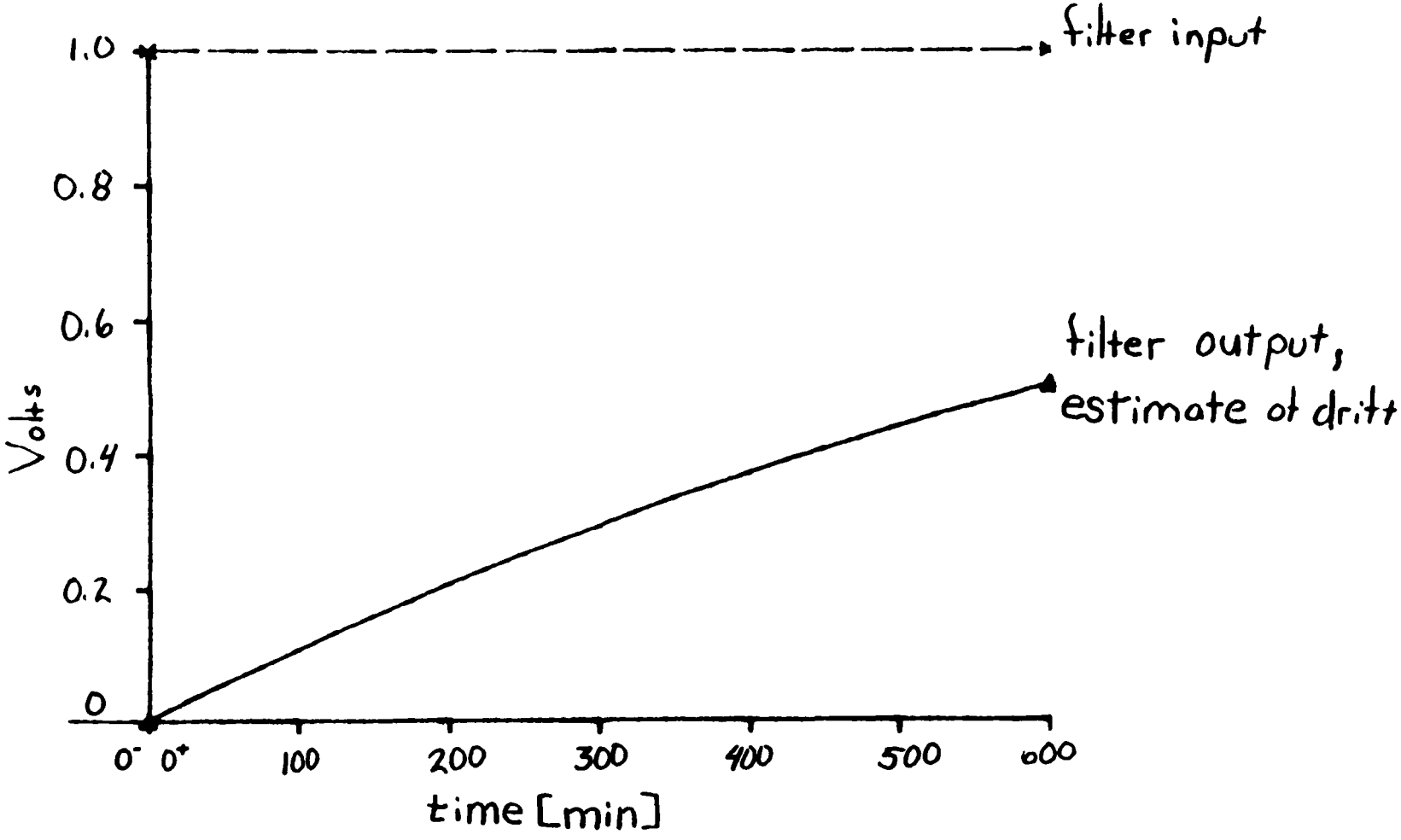


Fig 28 Error in estimating drift because of input signal. There is no drift in the input signal so any output represents an error in estimating the drift because of inclusion of some of the low frequency components of the input signal in the estimate of the drift. The filter used for these measurements had a time constant on the order of hours.

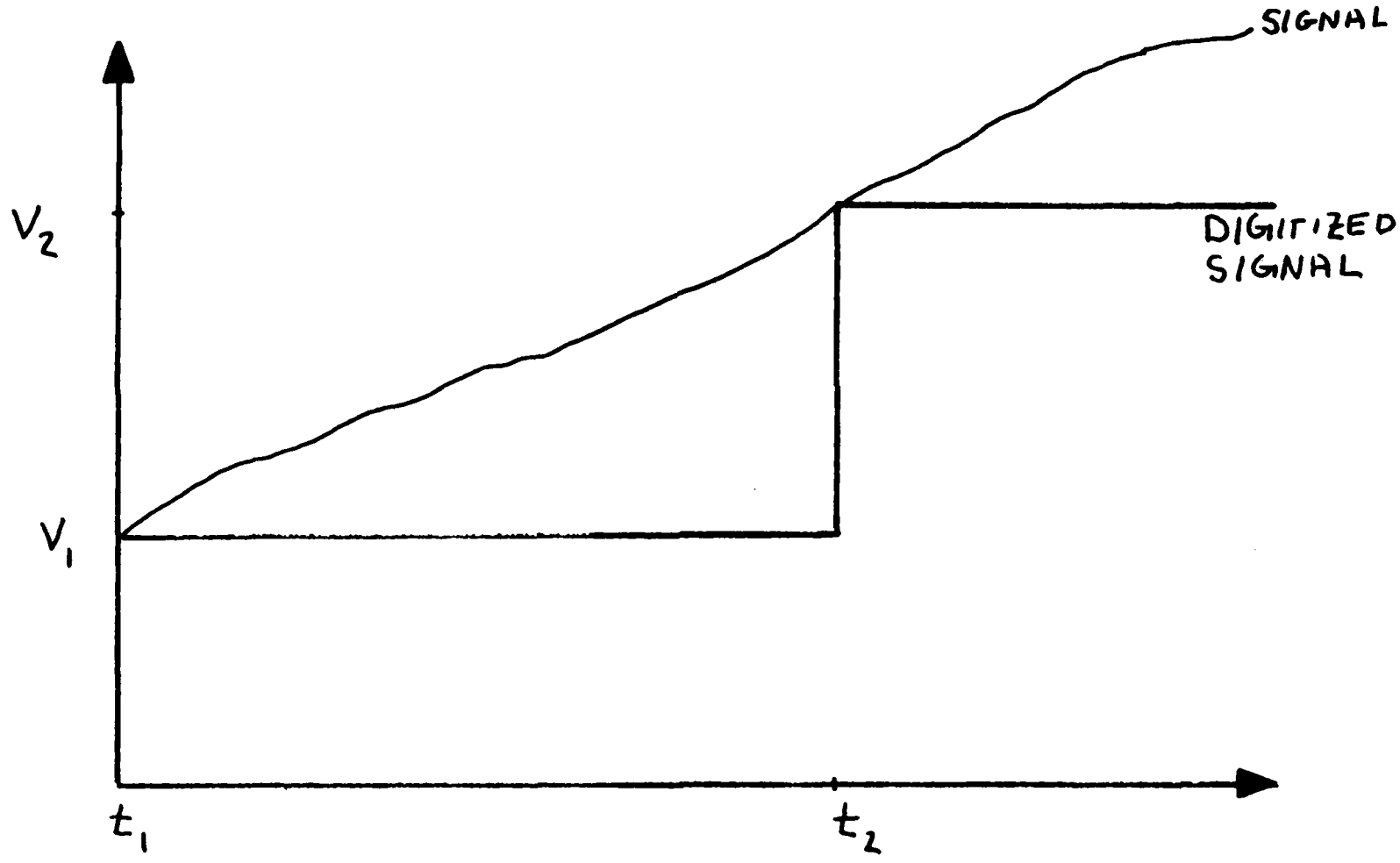


Fig 29 Quantization delay associated with A/D process. The time T2 - T1 represents the time needed for the A/D output, which is the filter input, to reflect any changes in the signal.

APPENDIX 1

Solution of FGFET Governing Equations

The specific technique used for numerical solution of these equations involves iterative calculation of possible operating points of the device until a point is found that simultaneously satisfies all of the describing equations to within a small tolerance. An example of determining a solution for a set of only two independant equations illustrates the algorithm used to calculate the I-V curve for the FGFET.

Consider the case of two independant equations in two variables, x and y. Such equations could be graphed in a two dimensional solution space with one variable on the ordinate axis and the other on the abscissa. (Fig A1) The point in the solution space where the curves intersect represents the point that satisfies both equations simultaneously. Thus, this point of intersection is the solution. A programmable algorithm to find the intersection of the curves representing the equations is possible if certain conditions are met. In the algorithm, an initial guess of the operating point is made by picking a point that falls on curve 1 as shown in Fig A2. This point has an x and a y value. For the same value of x, curve 2 has a different y value associated with it. The y value of this point can be mapped to another point on curve 1 with the same y value as the point on curve

2, but with a new x value. This value of x represents the first iteration in determining the value of x. In this way, using an x value to generate a y value and then using the y value to generate a new value of x, both values may get closer to the actual solution. Fig A2 shows the progression of approximate solutions as the calculated value approaches the actual solution.

The functions represented by Fig A1 are solvable using this algorithm because the approximations to the solution do converge to the actual solution. Convergance to the solution is not guarenteed by this algorithm. If the equations being solved were such that the y value for curve 2 changed a lot relative to changes in the y value of curve 1 for a change in the x value, the situation shown in Fig A3 would exist. After performing two iterations, the approximated solution is further from the actual solution than the initial guess. Thus, before applying this algorithm, it must be ascertained that the algorithm will converge as it did for the curves in Fig A2. An astute observer might note that in Fig A2 if the initial guess had been made on Curve 2 rather than on Curve 1, the algorithm would not converge to the solution. Similarly, in Fig A3 if the initial guess had been made on Curve 2, the approximations would converge to the solution. This fact indicates that the variable for which the initial guess is made is very important in determining a solution. From Figs A2 and A3, it can be seen that the relative slopes

of the monotonic curves at the point of intersection are important. To have convergance, the initial guess must be made on the curve that has a slope in the solution space of greater magnitude. [7]

When Vds<Vg-Vp, the describing equations are

$$V_g = \int_0^L V(y)\,dy \qquad (18)$$

$$V(y) = (V_g - V_p) + \sqrt{(V_g-V_p)^2 - \frac{2y}{L}(V_g-V_p)V_{DS} + \frac{y}{L}V_{DS}^2} \qquad (24)$$

$$I_D = \frac{h\mu_e \epsilon}{WL}\left[(V_g-V_p)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (22)$$

Though there are three equations, the first two do not depend on Id. The first two equations can be solved separately to determine a solution for V(y) and Vg, and then Id can be calculated from these values. In this case, there are two variables and two equations as in the example above. Moreover, Vg depends heavily on V(y) while V(y) depends mostly on the drain to source voltage. Thus, Vg should have the larger slope in the solution space, and the initial guess should be for a value of Vg. This guess should correspond to the situation in Fig A2 and the solution should converge. Verification of this fact will occur when the program is run. If the algorithm does not converge to the solution, it will give no answer - not a wrong one. It is possible that the equations have more than one solution. Graphically, this would be depicted as curves that

intersected at more than one point. In this solution could converge to the wrong intersection positive values of Vds can only be mapped to on value of Id. Thus, seeking I-V solutions in quadrant eliminates the possibility of choosin solution. The fact that this algorithm converges t solutions is demonstrated by the predicted I-V cur FGFET shown in Fig 10.

A similar approach is used for Vds>Vg-Vp. three equations to describe device operation in th

$$V_g = \frac{-2V_p + 3\delta(V_{ds} - V_o)}{4 - 3\delta} \qquad ($$

$$I_D = \frac{h\mu_e \epsilon}{W(1-\delta)} \left(\frac{(V_g - V_p)^2}{2} \right)$$

$$\delta = 1 - \exp\left[-\left(\frac{V_{DS} - (V_g - V_p)}{r_o I_D} \right. \right.$$

These equations can not be decoupled so they al solved together. If these equations were graphed dimensional solution space with each of the coord comprised of one of the independant varia intersection of the curves would represent the just as it did in two dimensions. Making an initia the value of two of the independant variabl calculation of the value of the third vari corresponds to the guessed values of the variables. Using the calculated value of the var

the guess of one of the other variables allows calculation of the remaining variable. The two calculated variables can be used to calculate the value of the third variable. Any two of the calculated variables can be used to calculate a new value for the third variable. This process, using two of the variables to update the value of the third, can be repeated, updating each variable in turn, until the solution converges. When the solution is reached, the variables will keep the same value no matter how many further iterations are performed. Thus, when the variables change very little between iterations, the values are very close to the actual solution. The program stops calculating iterations of the solutions once the variables change one percent or less between iterations.

Recall that in the derivation of Eqn 42 it was asssumed that δ was only a function of Vds and the use of the equation was restricted to situations where Vgs is constant. Notice that this condition is satisfied here since Id and Vgs are held constant when Eqn 42 is used to calculate a new value of δ.

There is one problem that has to be overcome in the implementation of this algorithm. The decision as to whether or not Vds<Vg-Vp can not be made directly since Vg is calculated in the algorithm. This calculation determines which set of equations is solved, so the result of the comparison must be known before the calculations can be

performed. Fortunately, application of physical reasoning yields a way to determine if Vds<Vg-Vp without calculating Vg first. The point where Vds=Vg-Vp corresponds to the point where the inversion layer extends all the way to the drain, but a depletion region is about to form. Thus, δ =0. Examination of Eqn 32

$$V_g = \frac{-2V_p + 3\delta(V_{DS} - V_p)}{4 - 3\delta} \qquad (32)$$

shows that in the limit as δ goes to zero, Vg=-1/2Vp. At Vds=Vg-Vp, Vg=-1/2Vp, so Vds=-3/2Vp. Thus for Vds<-3/2Vp, Vds<Vg-Vp,and for Vds>-3/2Vp, Vds>Vg-Vp.

A flowchart for the program implementing this algorithm is shown in Fig A4. The PASCAL code associated withthis algorithm is also shown. In this program,the integral in Eqn (18) is evaluated using a trapezoidal approximation to integration. The constants $\frac{h\mu_e\epsilon}{WL}$, that appear in several equations, have been combined into one constant, K. A value of K is determined from experimental measurements on an unmodified MOSFET. These constants also appear in Eqn (17), the formula for drain current in an unmodified MOSFET.

$$I_D = \frac{h\mu_e\epsilon}{WL}\left[(V_g - V_p)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (17)$$

Evaluating this expression at Vg-Vp=Vds,

$$I_D = K\frac{V_{DS}^2}{2}$$

or,

$$K = \frac{2 I_D}{V_{DS}^2} \qquad \text{for } V_{DS} = V_g - V_p$$

A value of Id at Vds=Vg-Vp can be read from the I-V plot shown in Fig 9. Note that Vp can also be determined directly from Fig 9. An I-V curve such as Fig 9 is experimentally obtained using a curve tracer.

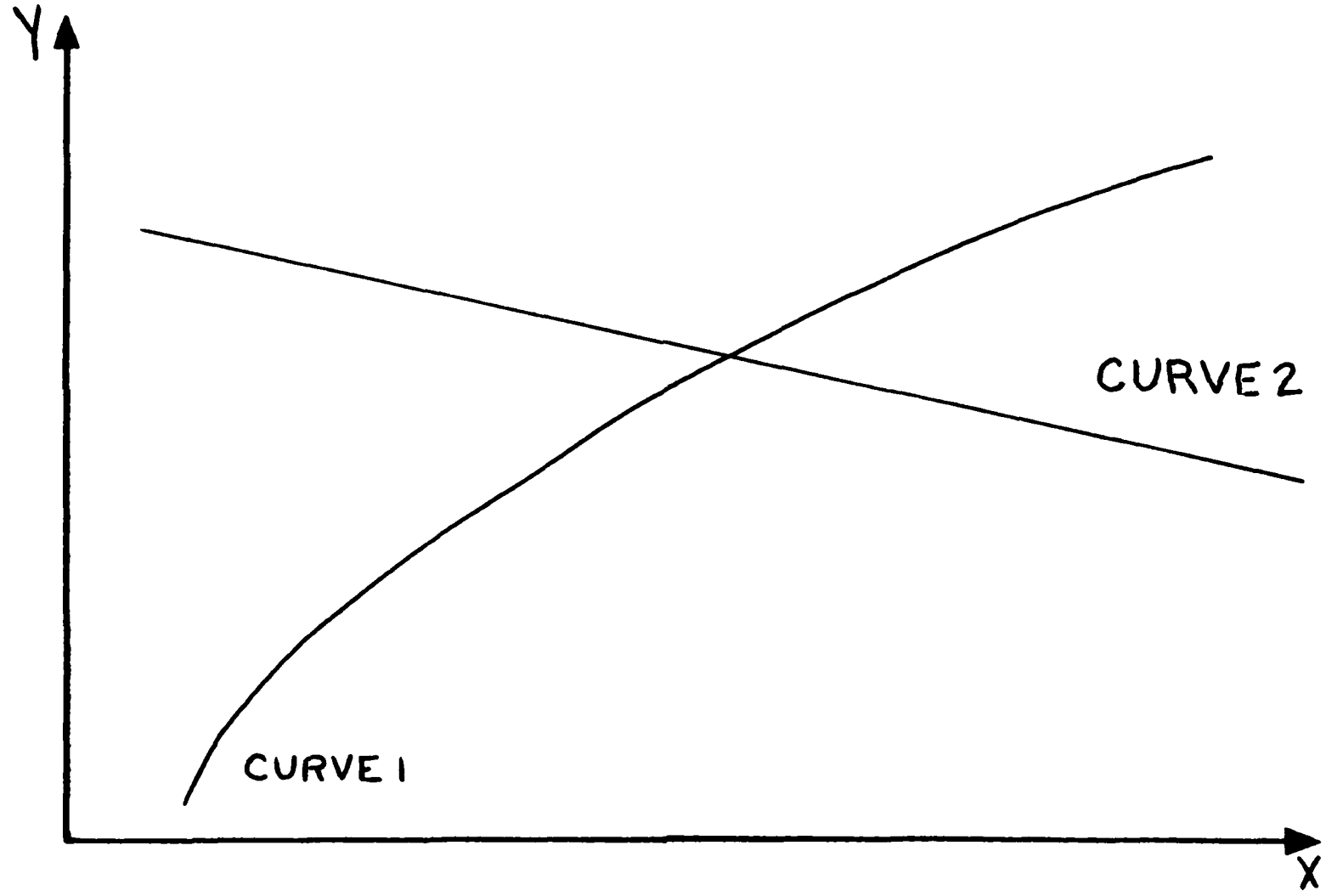


Fig A1 Curves representing two equations to be solved simultaneously

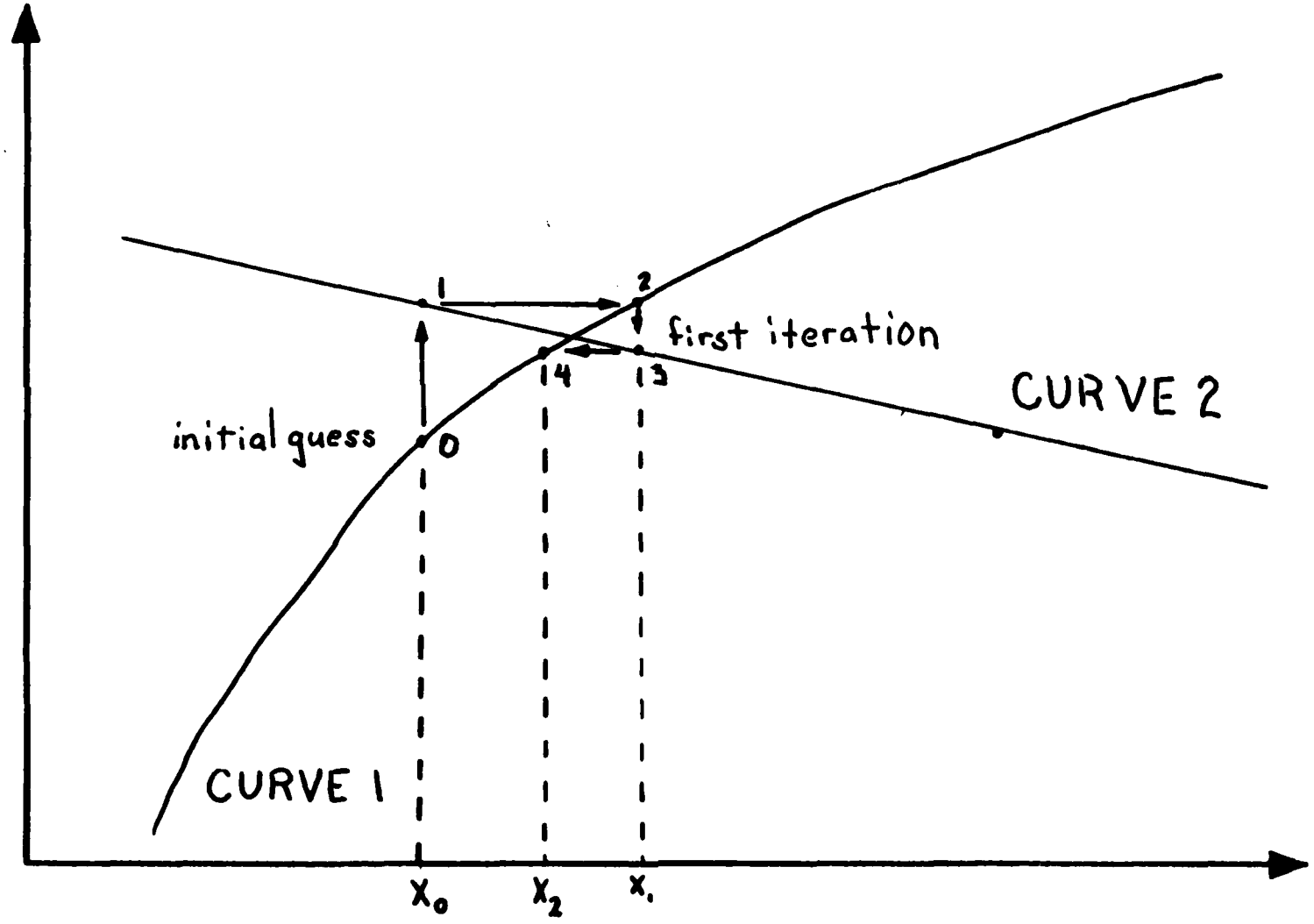


Fig A2 Curves with iterative solution converging

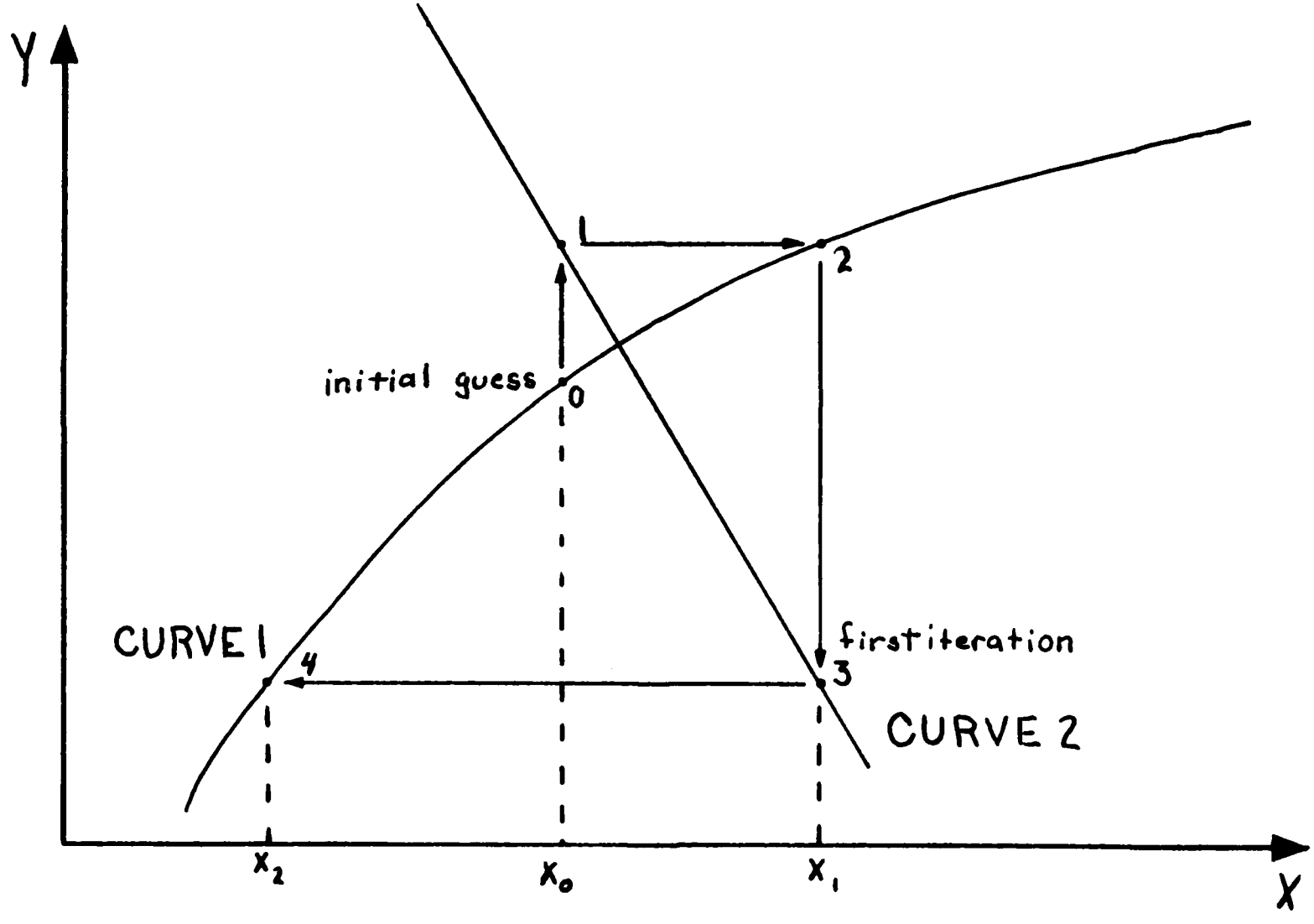


Fig A3 Curves with iterative solution diverging

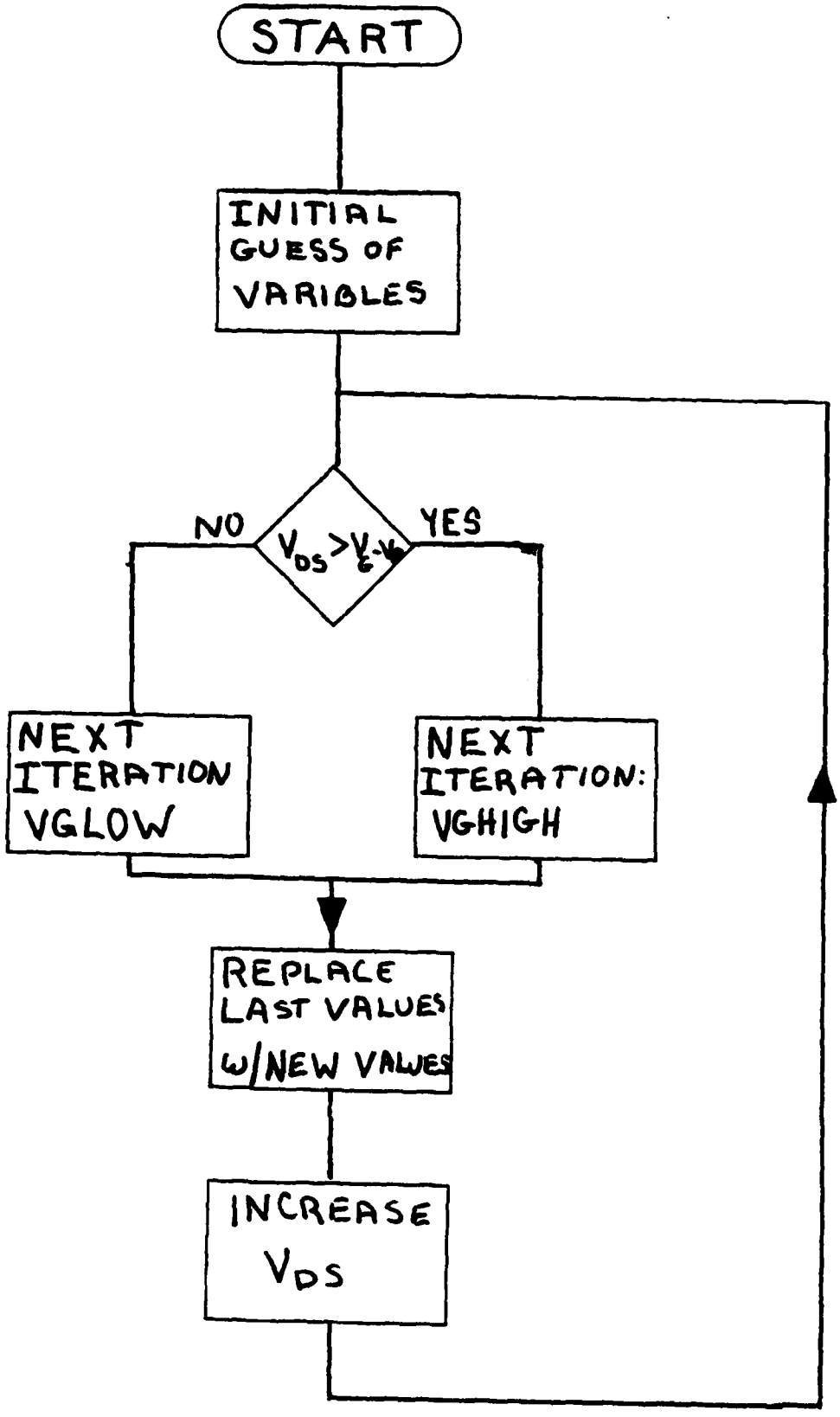


Fig A4a Flowchart of main program to calculate FGFET I-V curve

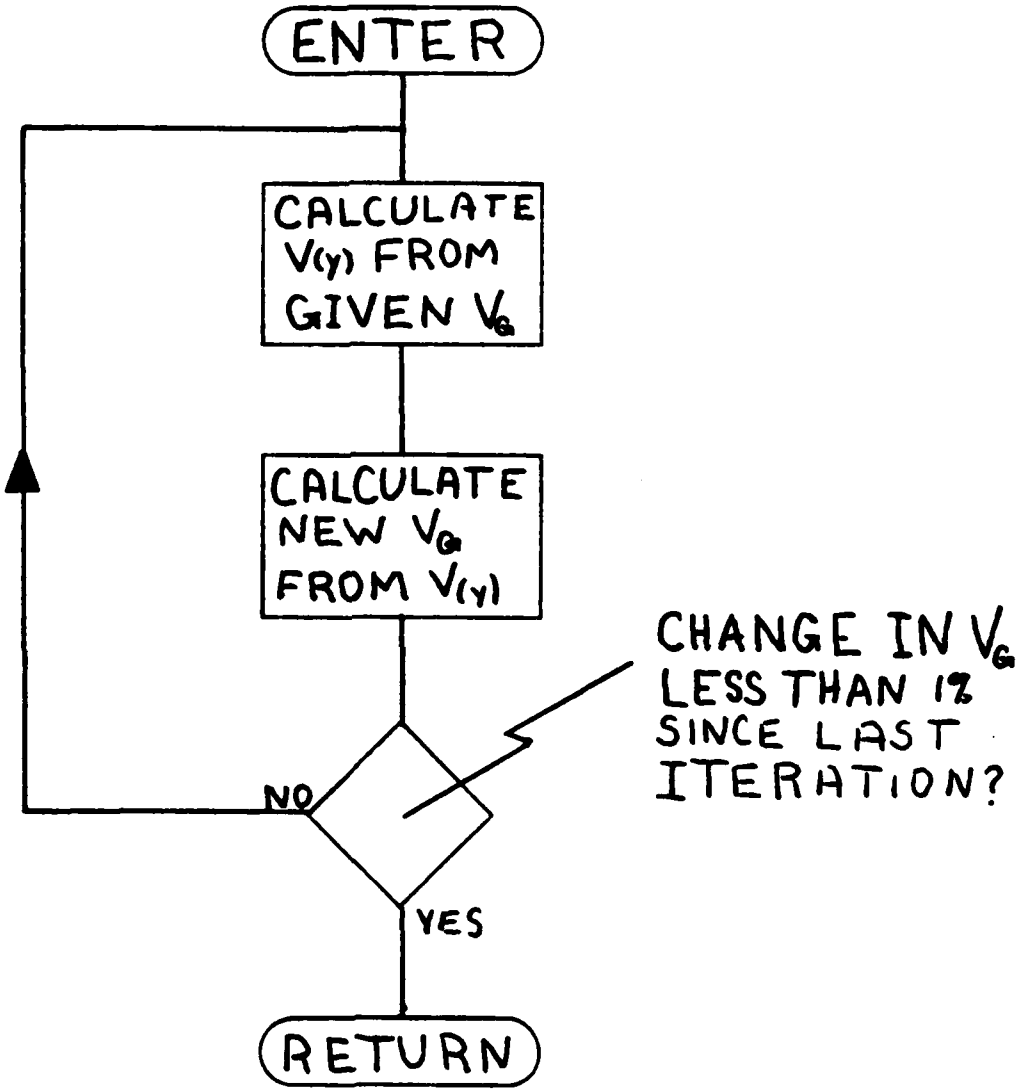


Fig A4b Flowchart of subprogram VGLOW to solve for a single point on the I-V curve when Vds < Vg - Vp

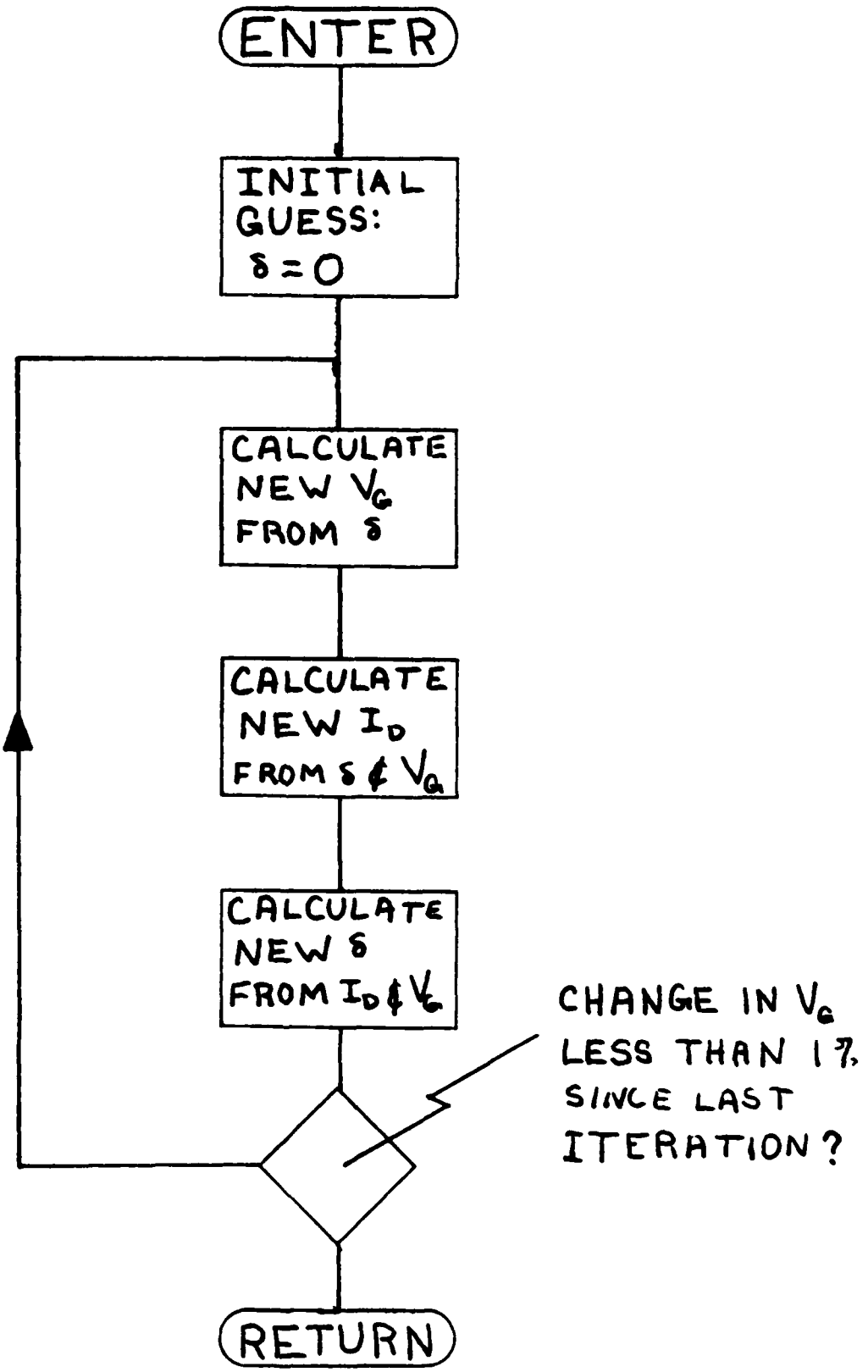


Fig A4c Flowchart of subprogram VGHIGH to solve for a single point of the FGFET I-V curve when Vds > Vg-Vp

PASACL Program to Solve FGFET Governing Equations

```
/file unit=(21,libout,name=atad1),dsname=atad1
/load pascal
(*$l-*)

program plotdata(input, output, console, atad1);

var  console, atad1 :text;
     vds, vgs, id, idplot, r0, k, vp, vdsmax :real;
     error :boolean;

procedure vglow(vds :real; var id, vgs :real);

const
  ynumstep = 100.0;
  dely = 0.01;

var
  vgsold :real;

  count :integer;

  error :boolean;

Function v(y:real) :real;
  begin
    v := (vgs - vp) - sqrt(Sqr(vgs - vp) - 2*y*(vgs - vp)*vds
         + y*sqr(vds))
  end;

function vg :real;

var
  v, vyl, x :real;
  Begin
    v := 0.0;
    x := 0.0;
    vyl := 0.0;
    while y < 1.0 do
      begin
        v := y + dely;
        if y < 1.0 then  x := x + dely*(v(y) + vyl)/2;
        if y < 1.0 then vyl := v(y);
      end; (*while*)
    vg := x
  end; (*function*)

Begin (*procedure body*)
  vgsold := 0;
  error := false;
  count := 0;
  while (abs(vgs-vgsold) > vgs/100) and (error = false) or (count =
    begin
      vgsold := vgs;
      vgs := vg;
      count := count + 1;
```

```
      if count > 100 then
       begin
        error := true;
        writeln('Error exit. 1% convergance not found in 100 iterati
        writeln('Program terminated in procedure vglow.')
       end (*if*)
    end; (*while*)
  id := k*((vgs - vp)*vds - sqr(vds)/2);
end; (*procedure*)


procedure vghigh(vds :real; var id, vgs :real);

var
vgsold, delta :real;

count :integer;

flag :boolean;

(*define functions*)

function vgsnew(delta :real) :real;
  begin
    vgsnew := (-2*vp + 3*delta*(vds - vp))/(4 - 3*delta);
    flag := true
  end; (*vgsnew*)

function idnew(delta, vgs :real) :real;
  begin
    idnew := k/(1 - delta)*sqr(vgs - vp)/2
  end; (*idnew*)

function deltanew(vgs, id :real) :real;
  begin
    deltanew := 1 - exp(-(vds - vgs + vp)/(r0*id))
  end; (*deltanew*)

(*procedure body*)
begin
  flag := false;

  count := 0;
  vgsold := vgs + 100;
  while (abs((vgs - vgsold)/vgsold) > 0.01) or (count = 1)
   and (error = false) do
    begin
      vgsold := vgs;
      if count > 100 then
        begin
          writeln('100 iterations performed without 1% convergance')
          writeln('program terminated in vghigh');
          error := true
        end; (*if*)
      if not flag then
       delta := 0;
      vgs := vgsnew(delta);
      id := idnew(delta, vgs);
```

```
      delta := deltanew(vgs, id);
      count := count + 1
    end; (*while*)
end;

begin(*main*)
  error := false;
  writeln;
  writeln(  'Program to claculate IV plot for FGFET.');
  writeln('Data in format suitable for plotting by telagraf is');
  writeln('stored in file atad1.');
  rewrite(atad1);
  writeln;
  writeln('r0 = ');
  reset(console);
  read(console, r0);
  writeln('k = ');
  reset(console);
  read(console, k);
  writeln('Vp = ');
  reset(console);
  read(console, vp);
  writeln('highest value of Vds to be plotted = ');
  reset(console);
  read(console, vdsmax);
  vds := 0;
  vgs := 0;
  id := 0;
  writeln(atad1, 'input data.');
  while (vds <= vdsmax) and (error=false) do
    begin
      if vds > -3/2*vp then vghigh(vds,id,vgs)
        else vglow(vds, id, vgs);
      idplot := id*1000;
      writeln(atad1, vds :10:4, ',', idplot :10:4);
      put(atad1);
      vds := vds + 0.1
    end; (*while*)
  writeln(atad1, 'end of data.');
  writeln('job completed. program terminated routinely.')
end.
```

APPENDIX 2

Design of Digital Lowpass Filter

The technique used to design the low pass filter uses a mapping of the analog s-plane into the digital z-plane. This technique allows an analog filter to be designed using standard analog filter design methods, and then, via the mapping, a suitable digital filter to be obtained. The mapping used here is called the bilinear transformation and is such that

$$z = \frac{1 + \left(\frac{T}{2}\right)s}{1 - \left(\frac{T}{2}\right)s}$$

where s represents complex frequency, T is the spacing between sampling that converts the analog signal into a digital sequence, and z is the independant variable in the z-transform domain. The bilinear transformation was chosen because the magnitude of the digital transfer function has the same shape as the magnitude of the analog transfer function, i.e. an analog low pass filter is converted to a digital low pass filter. However, the analog to digital transformation maps the entire $j\Omega$ axis (Ω represents analog frequency in rad/sec) into the unit circle of the z-plane. The unit circle is important because z-transfer functions evaluated on the unit circle in the z-plane yield the transfer function in terms of digital frequency because of the definition of the z-transform. The mapping is not

linear, so, although the shape of the transfer fun
the same, the digital frequency scale is distor
example, an analog filter might have a pass band th
times as long as its transition region. The digit
that results from application of the
transformation might have a transition region that
four times the length of the pass band. Fortuna
warping is predictable by the relationship

$$\omega = 2\tan^{-1}\left(\frac{\Omega T}{2}\right)$$

where ω is digital frequency. The critical frequenci
analog filter can be prewarped so that when the
axis is distorted by the transformation, the
digital filter has the desired critical frequencies

In this case, it is desired to design a digit
that has a cutoff for analog frequencies of $\frac{1}{T}$ ra
have an analog cutoff of $\frac{1}{T}$ rad/sec, the digital fi
have a cutoff at $\frac{T}{T}$ rad. Since it is known how t
frequncy axis will be warped in the transformatio
digital filter, the inverse of the warping functi
applied such that

$$\Omega_c = \frac{2}{T}\tan\left(\frac{\omega_c}{2}\right)$$

The analog filter that would give the right cutoff
when mapped into the digital plane thus would have
of

$$\Omega_c = \frac{2}{T}\tan\left(\frac{T}{2T}\right)$$

A simple first order analog low passfilter that has a cutoff of Ω_c is given by the transfer function

$$H(s) = \frac{\Omega_c}{s + \Omega_c}$$

The analog filter would thus be

$$H(s) = \frac{\frac{2}{T}\tan\left(\frac{T}{2T}\right)}{s + \frac{2}{T}\tan\left(\frac{T}{2T}\right)}$$

Mapped into the z-plane by the transformation

$$s = \frac{2}{T}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right)$$

the resulting filter has the transfer function

$$H(z) = \frac{(1 + z^{-1})\tan\left(\frac{T}{2T}\right)}{1 + \left[\frac{\tan\left(\frac{T}{2T}\right) - 1}{1 + \tan\left(\frac{T}{2T}\right)}\right] z^{-1}}$$

This digital filter has a cutoff of $\omega_c = \frac{1}{T}$. When the input to the digital filter is an analog signal sampled every T seconds, the filtered output, upon reconversion to analog, would have frequency components at $\frac{1}{T}$ rad/sec attenuated by 3dB. Higher analog frequencies would be attenuated more, and lower analog frequencies would be attenuated less.

The digital filter is of the form

$$H(z) = \frac{1 + b_1 z^{-1}}{1 + a_1 z^{-1}} = \frac{Y(z)}{X(z)}$$

This transfer function can be converted to a difference equation such that

$$y(n) = x(n) + b_1 x(n-1) - a_1 y(n-1)$$

resulting in an equation that can be implemented by a digital computer to realize the filter algorithm.[9]

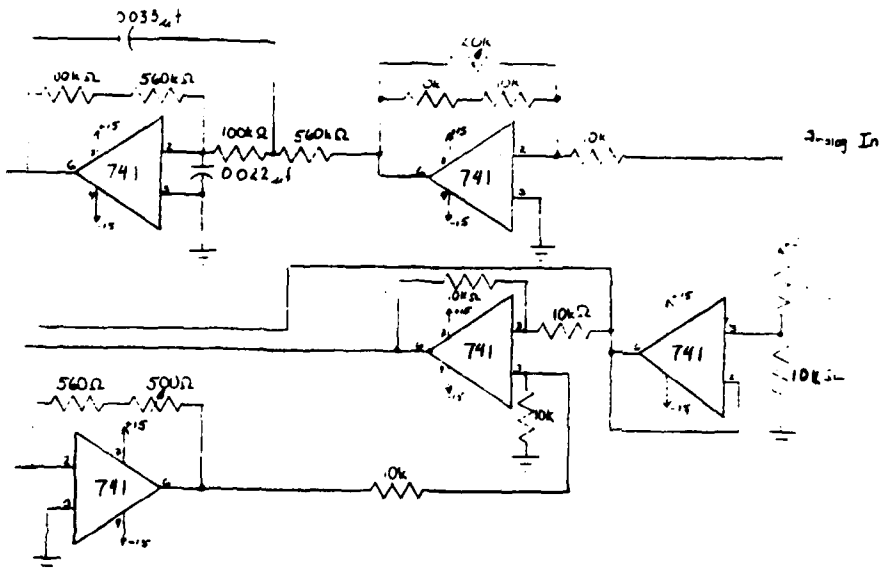
APPENDIX 3

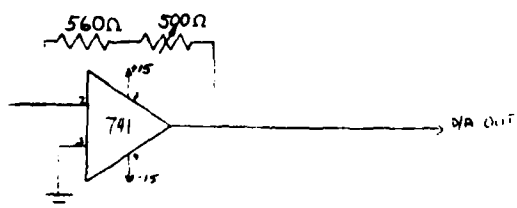
Hardware Implementation of Digital Filter

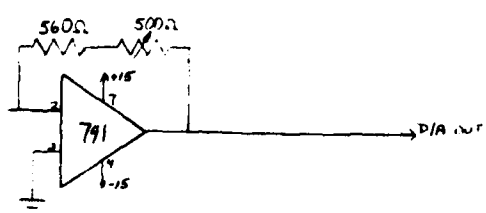
The digital filter equation of Appendix 2 is implemented in a Radio Shack TRS-80 Color Computer using the BASIC command interpreter residing in the computer ROM. This computer was chosen because of its availability and cost. The bus lines are accessed through the computer's cartridge port, allowing the computer to be easily interfaced with an external I/O board. Interface to the computer bus is accomplished with an 8255 PPI chip. The I/O board, which is shown in the accompanying schematic, is mapped into memory an the page FF40 to FF5F (Hex) because this page is decoded by an existing line on the TRS-80 bus, the Spare Select Signal (SCS). Output from the computer is accomplished through port B of the 8255 and is latched by the data latches. Data is multiplexed to any of the three output D/A converters by control signals from Port C, which serves as the control register for all functions on the I/O board. The bits of port C may be set or reset individually, allowing them to generate eight independant control signals.

Port B is at memory location 65345 (decimal) and Port A is at location 65344. Input from the A/D passes through Port A when the appropriate signals are generated by setting or resetting the control lines through Port C. The several bits of Port C are set or reset by writting the appropriate word

to the control register, which is mapped at 65347 (decimal). The A/D is preceded by a sample and hold and an analog low pass filter. The full scale range of the A/D is adjustable by means of a potentiometer. The output of the potentiometer represents one half of the dynamic range of the A/D. The range of input voltages overwhich the A/D operates can also be controlled in software, since one of the D/A outputs is dedicated to adjusting the reference value of the A/D. The output of this D/A is offset by one half of the A/D full scale value, making the dynamic range of the A/D from Vref-1/2Full Scale to Vref+1/2Full Scale.

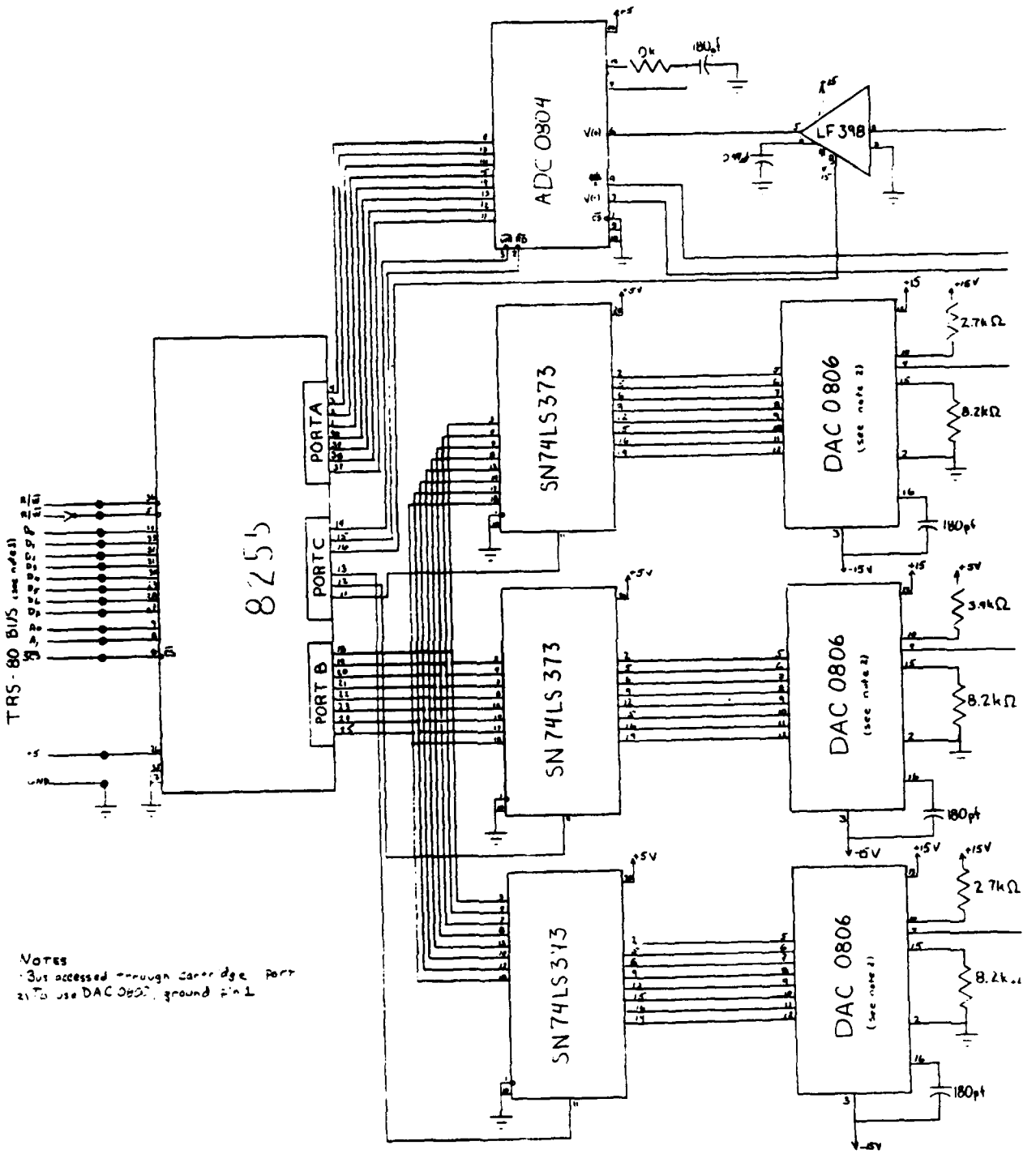






TRS-80 COLOR COMPUTER
I/O BOARD

August 15, 1983 E. T. Walsh



Notes
- Bus accessed through card edge Port
2) To use DAC 0807, ground pin 1

APPENDIX 4

Measurement of Gate Voltage Decay

Time constant measurements for gate voltage decay were made by recording the FGFET I-V curve as displayed on a curve tracer. The drain to source voltage supplied by the curve tracer is a rectified 60 Hz sine wave. Though this signal is continuously changing, it has a constant dc component. The gate pad will charge to the same value as it would were a true DC signal with the same value to be applied from drain to source. In Fig A5 is shown the curve tracer display recorded at increments in time. If the plot of Id vs. Vds with Vgs as a parameter is made of the MOSFET before the gate lead is severed, the value of Vg at any point on the curve in Fig A5 can be determined because the unmodified curve allows Vg to be determined as a function of Id and Vds. The DC components of these calculated gate voltages are shown in Fig A6. From these measurements, which are plotted semilogarithmicaly with time, it can be seen that the gate voltage decays exponentially towards the steady state value determined by resistive linking of the gate pad to drain, source, and substrate. This particular measurement indicates that the FGFET under test has a time constant of about 2.6 hours.

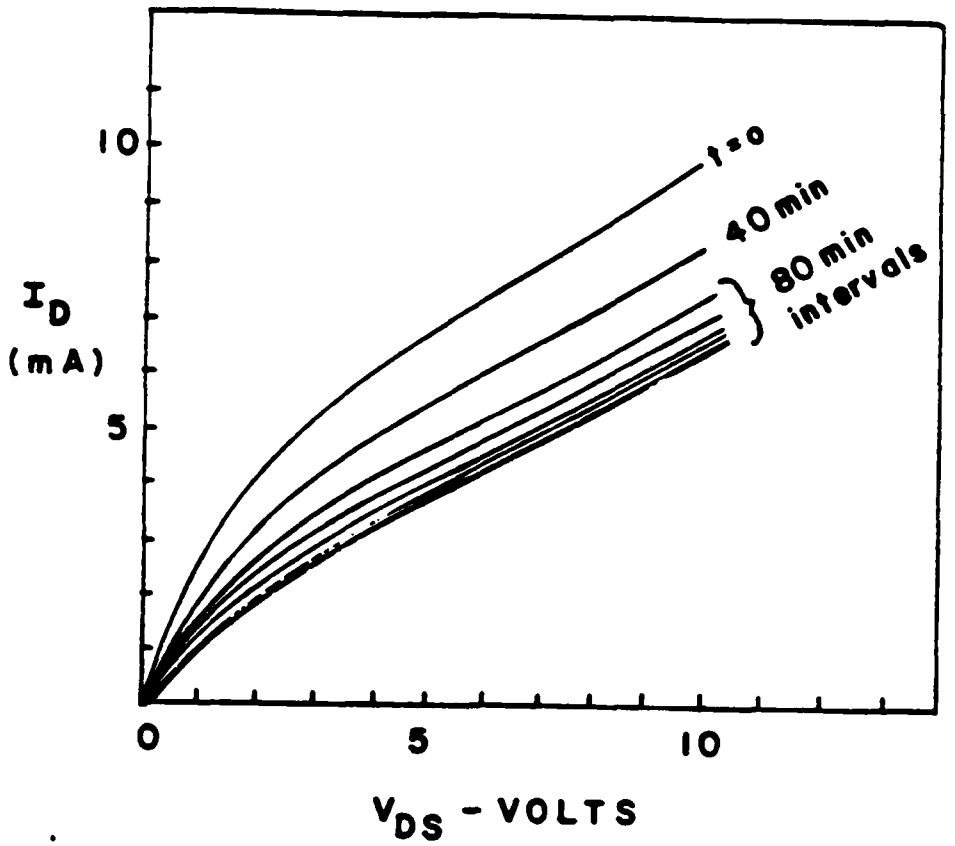


Fig A5 Change in FGFET characteristic curve as the dc component of gate voltage decays ti its steady state value

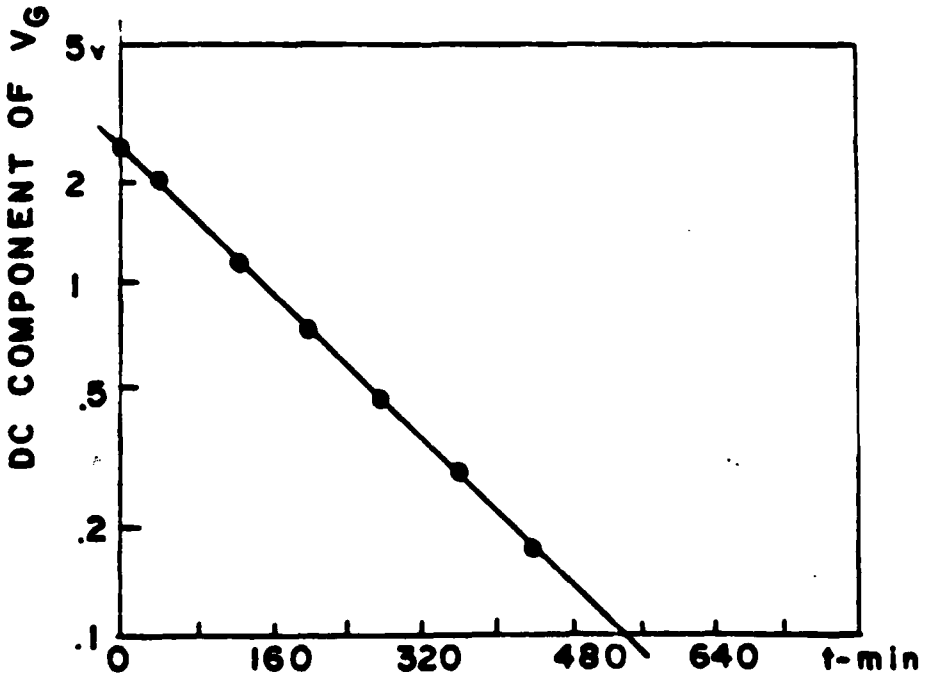


Fig A6 Decay of dc component of gate voltage showing the exponential decay with a time constant of about 2.6 hours

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